



APPLICATION NOTE 5.12

ULTRA I/O CMOS RAM BANK SWITCHING CONSIDERATIONS WITH SMI AND RUNTIME APPLICATION SOFTWARE

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OEM designers have combined System Management Mode processor features and the extended lockable 128 bytes of CMOS RAM in the FDC37C93X to add extensive power management features to their motherboard designs. Other data in the extended non-volatile RAM is used by OEM configuration and setup applications.

Care must be taken in this software to avoid a conflict that can occur when RTC IRQ8 interrupt handlers are called while the upper 128 byte block is selected. When the bank has been switched, the RTC registers 0x00-0x0D are actually replaced with RAM locations 0x80-0x8D.

If the RTC generates an interrupt when the upper bank is selected, the interrupt handler will be unaware of this and get erroneous data returned from these locations. This can cause serious system integrity problems since this software rightly assumes that these registers at 0x70 and 0x71 are always available.

The intended use of the extended 128 bytes was that it would be used only during POST and even locked out after that (see page 155 of the FDC37C93X data sheet, revised 4/21/95), and this situation would not normally be a problem.

However, if runtime OS or other code must enter the FDC37C93X configuration mode and access this memory, it is recommended that IRQ8 be disabled until the lower bank is readable so that periodic IRQ8s cannot occur when the RTC is masked by the upper RAM block. This may cause timers and counters to become inaccurate during these accesses, but it is far superior to the machine crashing. If the periodic IRQ8s are critical and cannot be missed at any time, then system designers should limit runtime data to the lower 112 bytes, and configuration information to the upper block.

The following is a recommended pseudo coding example for any software that selects the upper block of CMOS any time AFTER boot. All values in hex, FDC37C93X config. base assumed at 0x3F0.

```
; BEGIN APPLICATION THAT ACCESSES UPPER 128 BYTES OF CMOS
```

```
WRITE 3F0,55  
WRITE 3F0,55 ;ENTER CONFIGURATION MODE
```

```
WRITE 3F0,07  
WRITE 3F1,06 ;SELECT RTC LOGICAL BLOCK
```

```
WRITE 3F0,70 ;*****IMPORTANT: MUST PRECEDE BLOCK SWITCH  
WRITE 3F1,00 ;DISABLE RTC IRQ8  
;(MUST HAVE HARDWARE PULLUP ON IRQ8)  
WRITE 3F0,F0  
WRITE 3F1,80 ;SELECT UPPER 128 BYTE BLOCK
```

WRITE 70,INDEX
R/W 71,DATA ;MODIFY DESIRED LOCATIONS IN UPPER CMOS RAM

WRITE 3F0,F0
WRITE 3F1,00 ;RETURN TO LOWER 128 BYTE BLOCK

WRITE 3F0,70 ;*****IMPORTANT: MUST FOLLOW BLOCK SWITCH BACK
WRITE 3F1,08 ;REENABLE RTC IRQ8

WRITE 3F0,AA ;EXIT CONFIGURATION MODE



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