



## **REAL TIME CLOCK CONSIDERATIONS FOR SMSC ULTRA I/O DEVICES**

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The SMSC DS1287/MC146818 Register Compatible RTC core used in the FDC37C93X has an extraordinarily low power, high impedance 32KHz oscillator (<1uA) that can help reduce CMOS battery cost. Some applications have even used an inexpensive 1F supercap to replace the battery entirely.

There are obvious physical differences between the SMSC RTC and the DS1287 (the DS1287 includes a battery and crystal), and the SMSC RTC has functional differences with the MC146818 as well, including 256 bytes of NVRAM as opposed to the original 64 bytes. These differences and other advantages are discussed here. The FDC37C93X RTC is register compatible with the above standards, and all data sheet functions have been completely verified by SMSC, as well as other customers using the same RTC core in other parts.

### **FUNCTIONAL ISSUES:**

- 1) In BCD Mode, the SMSC RTC does not allow invalid values to be stored in time and alarm registers. (i.e. values above 59 cannot be written in the minutes and seconds registers.)
- 2) The Update-In-Progress bit is clocked rather than static, and will freeze if the RTC Oscillator is disabled. RTC Config Register A must have the RTC enabled before the UIP bit is valid. *(The RTC MUST be activated in the PnP configuration registers, and then enabled in Register A before it can be used).*
- 3) The DS1287A has a RAMCLR pin to set all bits in CMOS to a "1". The DS1287 does not have such a pin and the FDC37C93X does not have the pin budget for such a function either. Some users have disconnected the VBAT pin momentarily and observed a regular setting or resetting of the CMOS which is useful for invalidating the CMOS checksum so that BIOS will restore default values. This is not specified in the data sheet.

A more reliable extension of this, also used by other customers, is to check a GP input jumper and clear CMOS if the jumper is in. Another possibility is to check the keyboard at boot for a CMOS clear ctl-shft-alt-etc sequence.

- 4) The FDC37C93x is a Plug-and-Play part that powers-up 100% disabled, including RTC and keyboard functions. While the blocks still operate internally, they do not respond to bus accesses until they are enabled in configuration, as per the PnP 1.0a specification. This allows non-PnP core chipset RTCs to startup without conflict, if present. It also allows the placement of an alternate 8042 that takes precedence if populated.

Since previous core architectures typically accessed the keyboard controller and RTC through the local ROM BIOS XD bus, care should be taken to insure that these core hooks are disabled before the Ultra I/O blocks are enabled to avoid an SD bus conflict.

### **PHYSICAL ISSUES:**

- 1) Since older RTCs did not have the internal FET switches for transferring from VBAT to VCC, some legacy circuits used external discrete switching circuits. A protection diode and resistor were used in these circuits for UL approval to assure that a misoriented battery would not reverse bias the discrete switching circuit and cause a fire. The SMSC RTC does not need this type of protection (see Eval Board), but if it is used, a 0.1uF bypass cap from pin 121 to ground should be used to prevent any problems with the internal switching voltage comparators.
- 2) XTAL1, pin 122 is labeled as an ICLK buffer in the data sheet. This is incorrect. This input is expected to run off of a crystal only, and any other drive circuit could overload the amplifier and damage the chip.
- 3) The 1M resistor has been added to lower XTAL1's input impedance and make it less susceptible to noise. The 1 Meg value was chosen to provide a DC bias while drawing little excess current (20nA). Lower values could be used but I<sub>bat</sub> will increase (a few nA/Meg). Please see FDC37C93X Revision E section below.

### **LAYOUT ISSUES:**

Reasonable care must be taken during layout and routing of the RTC circuit to protect the sensitive oscillator. Most importantly, stray signal coupling must be reduced by avoiding the close routing of other PCB signals adjacent to the XTAL1 and XTAL2 inputs. This can be accomplished with a separate single-point PCB ground plane well, or with a top-layer ground guard. The attached example layout is a single layer ground guard implementation that isolates the XTAL inputs without modifying the ground plane or backside routing layer.

The load capacitors are seen by the crystal as two capacitors in series and should be approximately 2 times the C<sub>0</sub> of the actual crystal used (C<sub>L</sub>=2C<sub>0</sub>). For example, a 7.5pF crystal should use two 15pF capacitors for proper loading. The 1 Meg resistor (see .6u TLM) creates a very low current to bias the XTAL1 input to ground and shunt any extraneous DC offset.

The ground guard should be directly connected to pin 123 which is the actual RTC isolated ground. The outside ring of the guard shunts adjacent signals to ground, and physically inhibits dissimilar signals from being auto-routed through the circuit. This layout can be oriented inline or perpendicular to the chip pins to fit the specific layout, but the lines should be kept as short as possible.

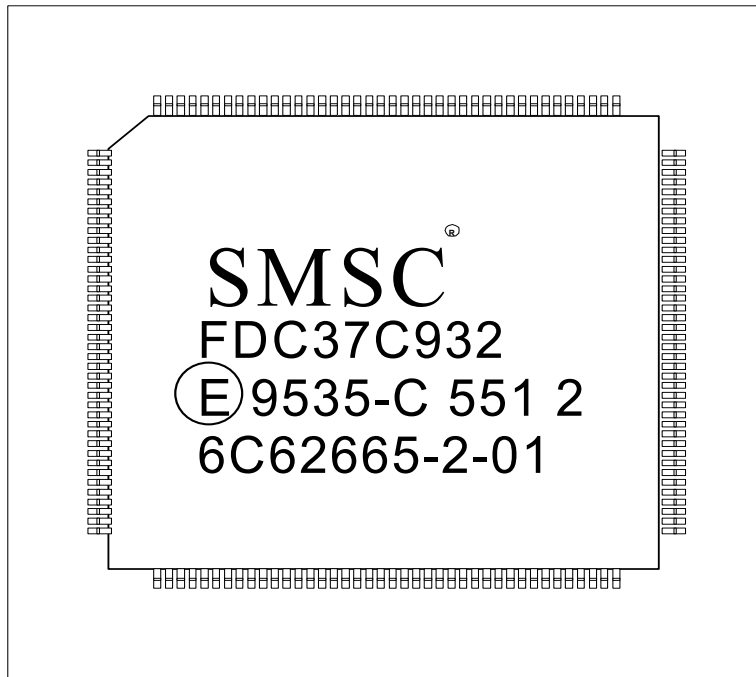
Ideally, the guard should encircle pins 122 and 124, but pad width usually does not allow this, so the guard should be terminated to the internal ground plane with a via at pin 123, and at the end of the guard next to pins 122 and 124.

### **.6u TLM Process - FDC37C93X Functional Revision E:**

There are some design issues that must be considered when designing and laying out the board with the SMSC FDC37C93X Ultra I/O controller in a .6u TLM (Triple Level Metal) process. This document will discuss the slight difference with .6u TLM material and aid the designer in designing a board to accept all parts without any impact on the production process.

**When designing with the .6u TLM part you must not use the 1 Meg resistor that is normally required from pin 122 to ground.** A good design strategy is to design and layout the board to accommodate for the 1 Meg resistor, and depending on the chip used, either populate or unpopulate that resistor location.

Figure 1 shows an example of a .6u TLM part. Note the functional Revision E preceding the date code which indicates the .6u TLM process.



**Figure 1: Sample of the FDC37C93X (.6u TLM) chip**



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