

DIFFERENCES BETWEEN FDC37C669 AND FDC37C665GT/IR

By using the FDC37C669, the design will meet the **REQUIREMENTS** and **RECOMMENDATIONS** of **WINDOWS 95**. In particular, it provides the compatibility for multiple IRQs, multiple DMAs and input/output address relocation. In this document, the following assumptions are made: The FDC37C665GT/IR is used in PC/AT and ECP mode, and the system is 5V, 3.3V/5V or 3.3V. The dual footprint can be accomplished using only seven to ten jumpers.

Figure 1 illustrates the pins that have different functionality on the FDC37C665 and the FDC37C669. The following table lists the pins that differ:

PIN	FDC37C665GT/IR	FDC37C669
1	DENSEL	DRV DEN0
18	DRATE1	DRV DEN1
19	DRATE0	IRQ_A
20	X1/CLK1	CLK14
21	X2/CLK2	DRQ_A
22	IDED7	nDACK_A
23	nIDEENLO	IRQIN
24	nIDEENHI	nIDEEN/IRQ_H
25	nHDCS0	nHDCS0/IRRX2
26	nHDCS1	nHDCS1/IRTX2
27	nIOCS16	nCS
36	nDACK	nDACK_B
37	IRQ3	IRQ_C
38	IRQ4	IRQ_D
39	PINTR	IRQ_E
40	FINTR	IRQ_F
52	FDRQ	DRQ_B
94	DRV2/ADRx/PINTR2	DRV2/ADRx/IRQ_B
96	PDACK	nDACK_C
97	A10	A10
98	VIO (IR), PDIR (GT)	VIO
99	PDRQ	DRQ_C

A description of the functional differences for each pin follows.

- Pin 1: DENSEL (pin 1), DRATE1 (pin 18) and DRATE0 (pin 19) on the FDC37C665 map onto DRVDEN0 (pin 1) and DRVDEN1 (pin 18) for the FDC37C669. For standard operation, (i.e., 4/2/1 MB 3.5", 2/1 MB 5.25" FDDS and 2/1.6/1 MB 3.5" mode 3 drives) DRVDEN0 is connected to DENSEL and DRVDEN1 is connected to DRATE0. For other operation see CR1F in FDC37C669 data sheet.
- Pin 18: See pin 1.
- Pin 19: See pin 1. On the FDC37C669, this pin can be used for IRQ_A.
- Pin 20: On the FDC37C665, this is the external connection for a parallel resonant 24 MHz crystal. It is used in conjunction with pin 21. On the FDC37C669, this pin is the external connection to a single source 14.318 MHz clock.
- Pin 21: On the FDC37C665, this pin is used for the 24 MHz crystal. If an external clock is used, this pin is not connected. On the FDC37C669, this pin can be used for DRQ_A, DMA request A for byte transfers of data between the host and the chip. It is used in conjunction with pin 22, the DMA_A acknowledge.
- Pin 22: On the FDC37C665, this pin is IDE7, which is used for IDE interface. On the FDC37C669, this input has been removed from the chip. Therefore, this pin can be used as a DMA_A acknowledge if DRQ_A is used (see pin 21).
- Pin 23: On the FDC37C665, this pin is used as nIDEENLO, IDE low byte enable. On the FDC37C669, both this signal and IDEENHI (pin 23) have been replaced by nIDEEN (pin 24). Therefore, this pin can be used as IRQIN to steer an interrupt signal from an external device onto one of the eight IRQ outputs IRQA-H.
- Pin 24: On the FDC37C665, this pin is used as nIDEENHI, IDE high byte enable. On the FDC37C669, this signal was replaced by nIDEEN at this pin to control both the low and high bytes of the IDE interface.
- Pin 25: This pin is used as nHDCS0 on both chips when IDE is used (see Note 1).
- Pin 26: This pin is used as nHDCS1 on both chips when IDE is used (see Note 1).
- Pin 27: On the FDC37C665, this pin is used to indicate when IDE 16 bit transfers are to take place. However, all IDE transfers are allowed to be 16 bit. Therefore, on the FDC37C669, when enabled, it is used as an input for an external decoder circuit which is used to qualify address lines above A11. Thus the pin is either logically ORed with A11-A15, or connected to ground (if not used).
- Pin 36: This pin will correspond to the DACK on the FDC37C665 when pin 52 is configured on the FDC37C669 as described below (i.e., DRQ_B is selected for the FDC).
- Pin 37: This pin on the FDC37C669 will correspond to the FDC37C665 when CR28 is set properly. If IRQ3 is used for serial port 1 (PSP), select IRQ_C for serial port 1 by setting bits 7:4 to 0011. If IRQ3 is used for serial port 2 (SSP), select IRQ_C for serial port 2 by setting bits 3:0 to 0011.
- Pin 38: This pin on the FDC37C669 will correspond to the FDC37C665 when CR28 is set properly. If IRQ4 is used for serial port 1 (PSP), select IRQ_D for serial port 1 by setting bits 7:4 to 0100. If IRQ4 is used for serial port 2 (SSP), select IRQ_D for serial port 2 by setting bits 3:0 to 0100.
- Pin 39: To make this pin correspond to PINTR in the FDC37C665, select IRQ_E for the parallel port IRQ on the FDC37C669. Set bits 3:0 in CR27 to be 0101.
- Pin 40: To make this pin correspond to FINTR in the FDC37C665, select IRQ_F for the FDC IRQ on the FDC37C669. Set bits 7:4 in CR27 to be 0110.
- Pin 52: To make this pin correspond to FDRQ in the FDC37C665, select DRQ_B (DMA request B) for the FDC on the FDC37C669. Set bits 7:4 in CR26 to be 0010.
- Pin 94: This pin is used in the same way on both the FDC37C665 and the FDC37C669 for the three functions DRV2, ADRx and PINTR2 (see CR03).
- Pin 96: This pin corresponds to PDACK in the FDC37C665 when DRQ_C is selected for the parallel port on the FDC37C669. See pin 99.
- Pin 97: This pin is used for A10 in both chips.
- Pin 98: The FDC37C669 supports 5V, 3.3V/5V and 3.3V operation, as does the FDC37C665IR through VIO on this pin. There is no PDIR on the FDC37C669 as there is on the FDC37C665GT. The table below illustrates the use of VIO in conjunction with VCC for the different operating voltages.

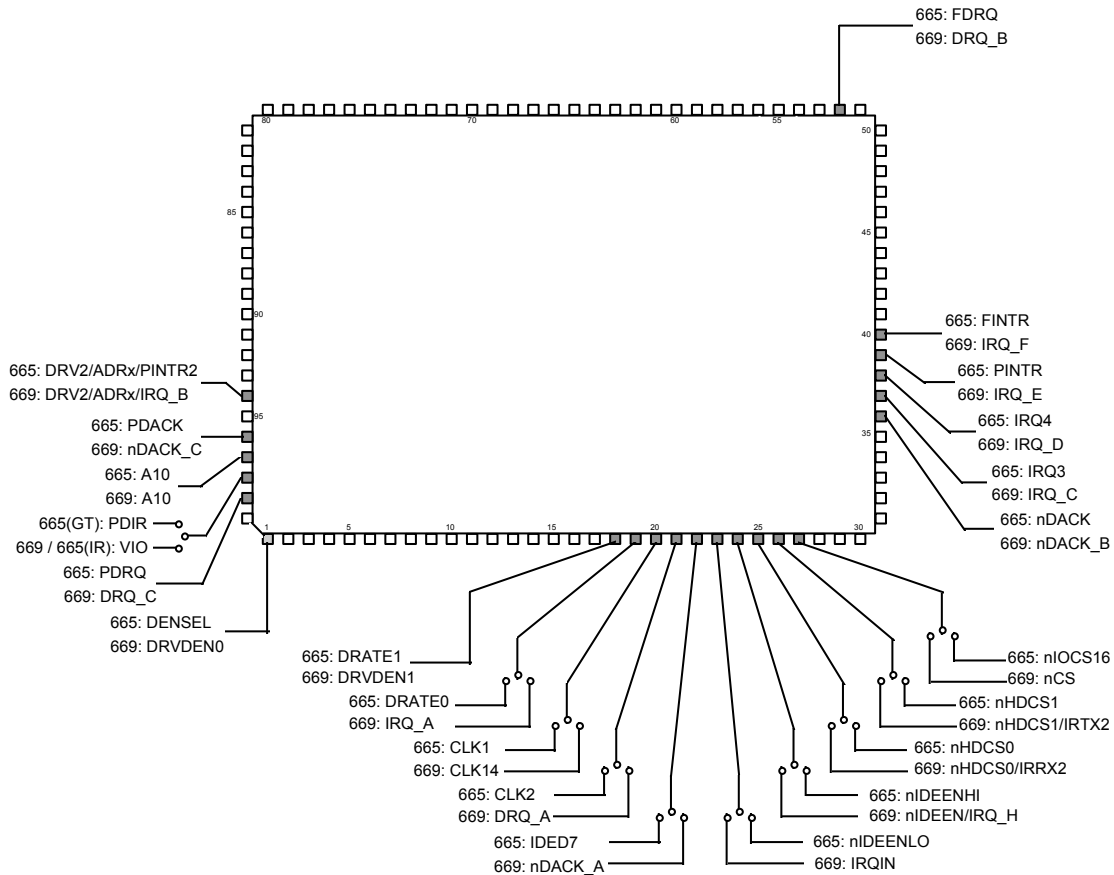
Operating Voltage	VCC	VIO
5V	5V	5V
3.3V/5V	3.3V	5V
3.3V	3.3V	3.3V

Pin 99: To make this pin correspond to PDRQ in the FDC37C665, select DRQ_C (DMA request C) for the parallel port on the FDC37C669. Set bits 3:0 in CR26 to be 0011.

Note 1: If the IDE drive function is not used, the alternate functions can be used for pins 24-26 on the FDC37C669 i.e., IRQ_H, IRRX2 and IRTX2. If the IDE drive function is used, IDE bit 7 from the IDE drive must be buffered along with IDE bits 0-6 and controlled by IDEEN.

Note 2: The designer must evaluate the decoupling requirements. SMC recommends that decoupling capacitors be located close to all power and ground pins.

FIGURE 1 - FDC37C669 vs. FDC37C665GT/IR





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