



**WINDOWS '95 SOFTWARE CONFIGURABLE DMA/IRQ SELECTION
WITH FDC37C665GT/LV/IR 11 BIT ADDRESS DECODER**

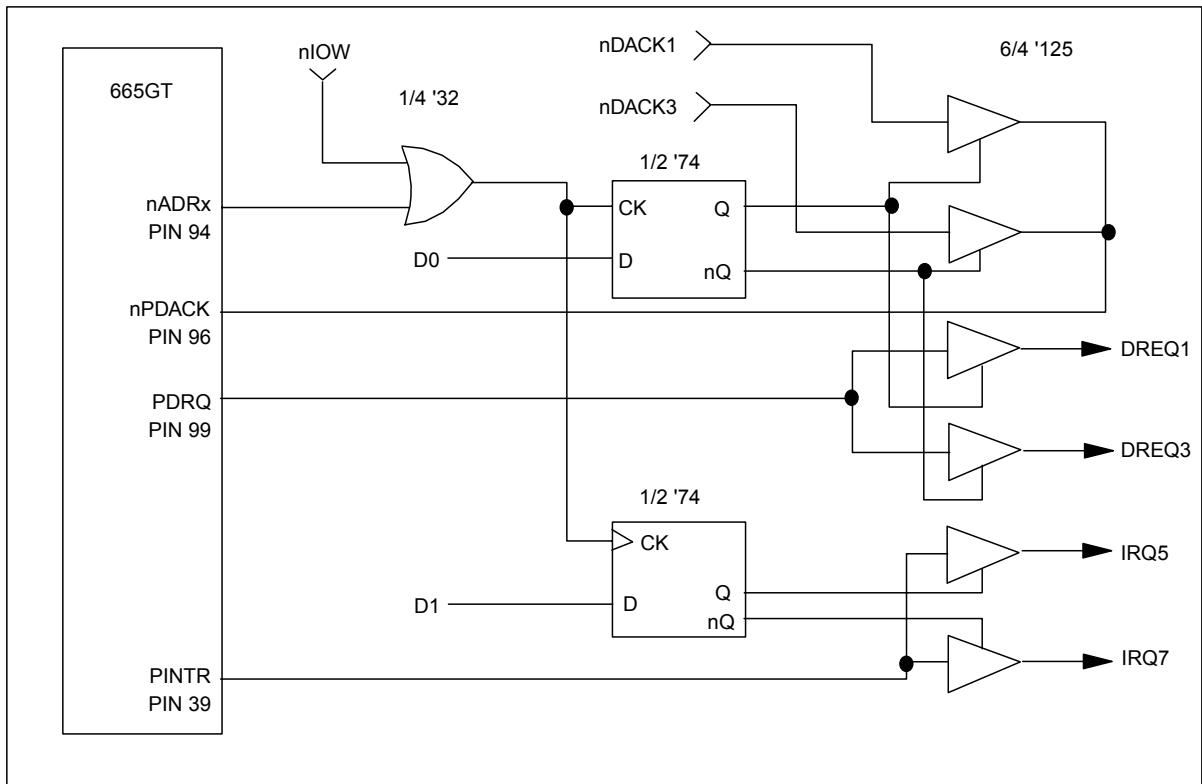


FIGURE 1

Note: This is only a simplified discrete example circuit. More integrated, less expensive implementations are possible.

FDC37C665GT/LV/IR IRQ/DMA CONFIGURATION:

1. Set CR8 and CR9 to desired unused 11-bit I/O port address
2. Enable ADRx decode output on pin 94 by setting CR3/bit 7 to 1 and CR3/bit 2 to 0.
3. Write to configuration bits D0 (DMA Select) and D1 (IRQ Select) for proper selection.

Figure 1 shows a 3-state buffer mux implementation. Appropriate logic family selection should be made to meet timing requirements. Figure 2 below shows an open collector implementation using 1 74X74 and 2 74X09s. *The open collector implementation should not be used if system DRQ or IRQ has pull-downs or ladder terminations.*

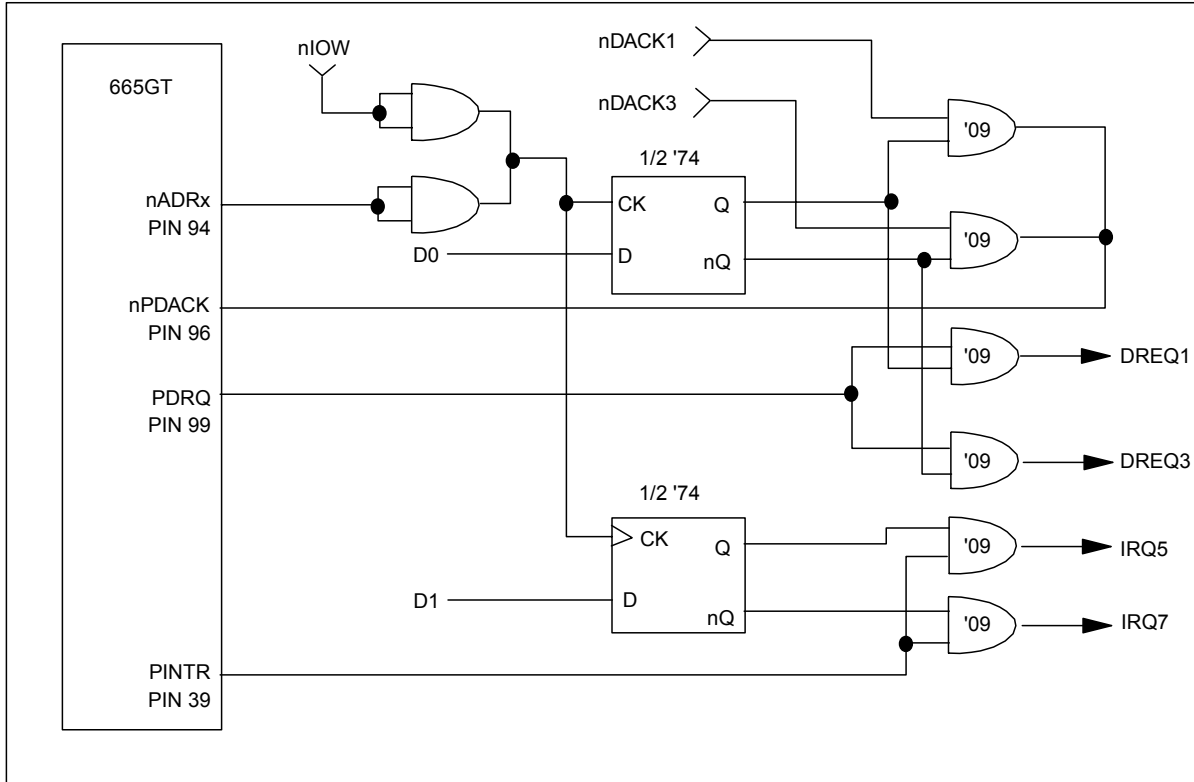


FIGURE 2

Note: Open collector '9 AND gate outputs require appropriate pullups.

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