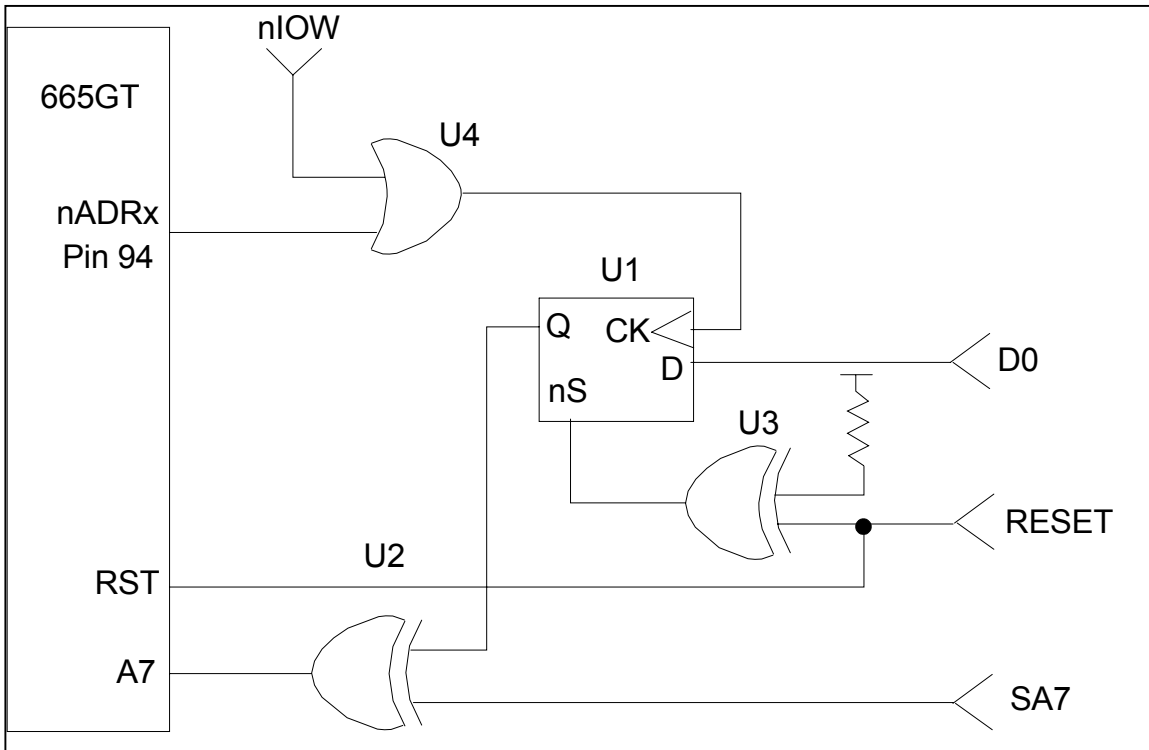


## ADDRESS RELOCATION OF SUPER I/O CONFIGURATION REGISTERS WITH THE FDC37C665GT/LV/IR

The FDC37C665 Super I/O is a software configurable device that replaces hardware jumpers with configuration registers for a "Plug-and-Play" type motherboard. The FDC37C666 series is designed for adapter card applications. The FDC37C666 series of parts are also software configurable, but give the designer hardware strapping options for the certain initial default values. However, options that are hardware strapped cannot be modified through software with the FDC37C666.

Two major applications require the software configurable features of two or more FDC37C665s to exist on the same ISA bus: laptops with docking stations, and "jumperless" adapter cards used with a motherboard that already uses a FDC37C665. Since both FDC37C665s will respond to configuration port 0x3F0, some other means of independent configuration is required. (The FDC37C666 does not present this conflict since it uses a <0x44,0x44> configuration sequence instead of <0x55,0x55> used by the FDC37C665).

The following schematic offers a way to allow the configuration registers of the secondary FDC37C665 (on the adapter or in the docking station) to appear at the alternate address available in the FDC37C666 (0x370 & 0x371, instead of 0x3F0 & 0x3F1). Theory of operation is as follows:



On power up, or during RESET, RESET must be "high" for at least 500ns. U3 is used as an inverter (since at least one 74X86 must be used) to force flip - flop U1 to a known state of Q = 1 on RESET.

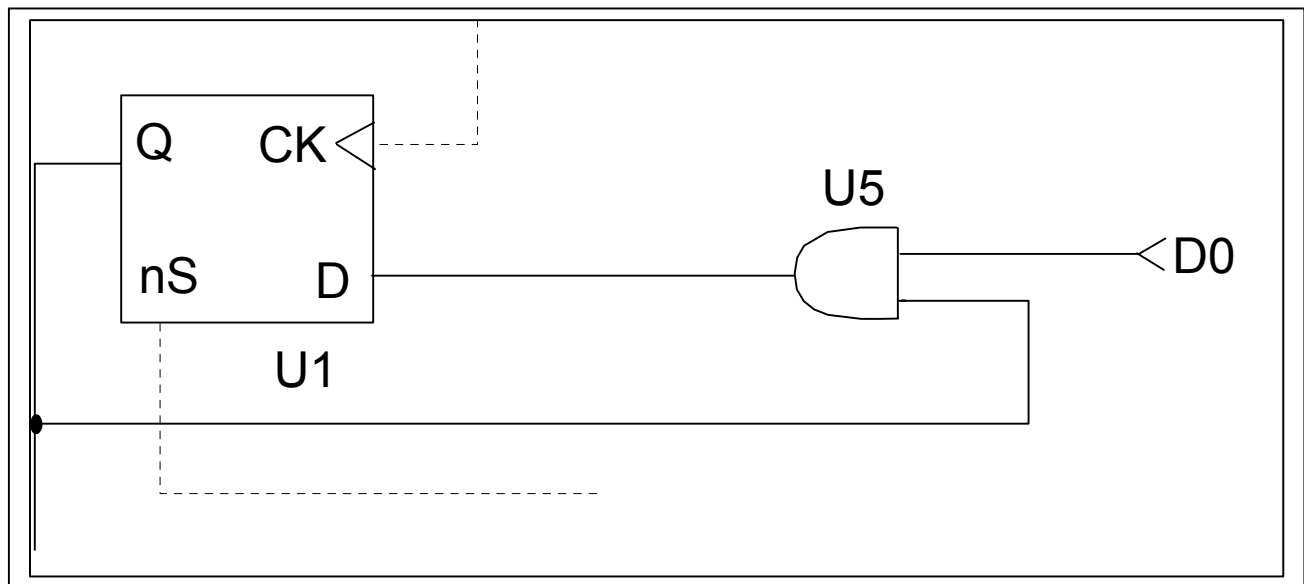
When Q = 1, U2 becomes an inverter and inverts the FDC37C665's SA7 input. This makes system address 0x370 and 0x371, appear to the FDC37C665 as 0x3F0 and 0x3F1. At this point, the main FDC37C665 configuration registers reside at 0x3FX, and the secondary FDC37C665 configuration registers reside at 0x37X.

The secondary FDC37C665 functional blocks should then be configured to non-conflicting values. Also, CR8 and CR9 should be set to an unused 11 - bit I/O address. This will be the "Alternate FDC37C665 Config Enable" port. This port decode can then be enabled by setting CR3/bit 7 to 1, and CR3/bit 2 to 0. When configuration is complete, exit by writing an <0xAA> to 0x370, and a 0x00 to the "Alternate FDC37C665 Config Enable" port. NOTE: Writes to this port must take into account the toggled A7 bit, (i.e. setting the port to 0x300, would require a write to 0x380 when Q = 1 and 0x300 when Q = 0).

To reenter configuration mode, simply write a 0x01 to the "Alternate FDC37C665 Config Enable" port, and then <0x55,0x55> to 0x370.

Careful selection of the "Alternate FDC37C665 Config Enable" port address is imperative, since accidental initiation of Config Mode will scramble all normal addressing to the second FDC37C665. For more security, a CRC bit or qualified byte value could be passed into the flip - flop rather than just D0. Also, D can be tied to ground so that once config mode is exited, it cannot be reentered without resetting the computer.

If bits D1-Dxx are to be used for other configuration purposes (see IRQ/DMA selection, and Serial EEPROM application notes using the FDC37C665GT) then the one - shot Configuration mode can be accomplished with the following circuit. A write of 0x00 is required to exit configuration mode, as long as the " Alt Config" port is written with D0 = 1, configuration mode will continue.





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