



APPLICATION NOTE 6.5

CRITICAL GP I/O INITIALIZATION ON THE FDC37C93X Series of Ultra I/O's By Jeffrey Dunnihoo

The extensive configurability of the FDC37C93x, FDC37C93xPM, and FDC37C93xFR series of parts can cause difficulties with the use of GP I/O pins as outputs to control system board functions such as CPU clock PLLs, FLASH lockout, and other power management functions.

The basic tenet behind the 93x design is that all logical devices (there are 8 blocks on the 93x) come up 100% disabled and tri-stated where possible. This avoids any conflicts with non-PnP devices. All devices are also disabled during configuration mode. This avoids problems with Multi-register configurations (such as ASKIR/UART unit), where all changes must take effect at once to avoid unexpected intermediate results.

A problem can occur when GPI/O functions are altered from their initial INPUT (hi-impedance) state to active high or low outputs. The outputs must be enabled first before a preset value can be assigned. This can cause an unexpected level on a pin from the time the pin is enabled, to the time it is written to. If this is used to control a CPU clock select, it could cause the processor to hang!

The configuration section has a hidden mechanism for dealing with this. Page 114 of the 93x data sheet shows how Bit-1(Polarity) can be used during configuration mode to "preset" the value of the gpio output BEFORE it is enabled. The D type FF is reset to a low (0) on POR. Therefore, if you need the pin to initialize to a low (0) then Bit-1 should be a low (0). If you need the pin to start out at a high (1), then Bit-1 should be a 1.

CODE EXAMPLES

```
WCFG      MACRO      @INDEX,@VAL
           MOV        AL,@INDEX
           MOV        DX,3F0H
           OUT        DX,AL          ;IODLY
           MOV        AL,@VAL
           INC        DX
           OUT        DX,AL          ;IODLY
           ENDM
```

```

;ENTER CONFIG
    MOV    AL,55H
    MOV    DX,3F0H
    CLI
    OUT    DX,AL
    OUT    DX,AL
    STI
;
    WCFG 0E0H,02H           ;Setup GP10 as nFLASH_WE
    ;We want a FLASH_WE# output to initialize INACTIVE (hi)
    ;
    WCFG 0E1H,00H           ;Setup GP11 as TURBO_OUT
    ;We want a TURBO_OUT output to initialize INACTIVE (low)
;
;
;CONTINUE WITH OTHER 93x CONFIGURATION
;
;
;EXIT CONFIG
    MOV    AL,0AAH
    MOV    DX,3F0H
    OUT    DX,AL

; Now GP1.0 and GP1.1 can be simply considered as ON=1, OFF=0.
; To enable Flash writes, write a 1 to GP1.0
    MOV    AL,01H           ;GP1 INDEX
    OUT    0EAH,AL
    IN     AL,0EBH          ;READ/MODIFY/WRITE BIT[0] FOR GP1.0
    AND    AL,00000001b
    OUT    0EBH,AL

; To enable high speed Turbo clock mode, write a 1 to GP1.1
    MOV    AL,01H           ;GP1 INDEX
    OUT    0EAH,AL
    IN     AL,0EBH          ;READ/MODIFY/WRITE BIT[1] FOR GP1.1
    AND    AL,00000010b
    OUT    0EBH,AL

```

A weak pull-up, or pulldown should also be added to preserve the desired state from power-on till configuration.

Following configuration, the programming model for the pin should be considered as active = 1, inactive (default)=0 and no further consideration of the internal inverter should be given.

Another problem case occurs when a GPIO is switched from its default function to a critical alternate output function. For example, GP20 can be used as CPU_RESET, or with the included inverter, nCPU_RESET. Bit 4 of CR0xE8 enables this function, and Bit 1 can be used to invert it before it leaves the chip.

Therefore, using the same method described above, write a 0x10 to CR0xE8 to get CPU_RESET, and 0x12 to get nCPU_RESET. Note that enabling a mux and an inline inverter simultaneously can cause a momentary glitch since the switching speeds of these two blocks are not identical. Therefore it is usually necessary to enable these with the output buffer disabled, and then turning the buffer on after the glitch has settled internally. This can be done by keeping Bit 0 set and then clearing it. (i.e. Write a 0x13 and then a 0x12)

CODE EXAMPLES

```

;ENTER CONFIG
;
;
;
;
;           WCFG 0E8H,010H           ;Setup GP20 as RESET_OUT
;
;           ; - or -
;
;           WCFG 0E8H,013H           ;Setup GP20 as RESET_OUT#,
;                                     ;but keep output buffer disabled
temporarily
;           WCFG 0E8H,012H           ;Now enable output buffer
;
;
;CONTINUE WITH OTHER 93x CONFIGURATION
;
;
;
;EXIT CONFIG

```

The methods described above in this Application Note are equally applicable to the FDC37C93x, FDC37C93xPM, and FDC37C93xFR devices.



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