

CONSUMER IR PRIMER/MANUAL/SOFTWARE OUTLINE

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INTRODUCTION

Many of SMSC's Ultra and Super IO's contain an IRCC block. These blocks typically contain FIR (IRDA 1.1 HDLC,4PPM), SIR (ASK,IRDA 1.0), and Consumer IR blocks. The FDC37B77x contains a CIRCC block which includes advanced NEC framing detect logic and programmable wake-up events under standby power.

This application note is intended to provide a brief 'low-level' explanation of the Consumer portion of the Synchronous Communication Engine. Standard Consumer IR as well as our new NEC framing will be explained. Also included will be a manual for our in-house low level Consumer IR software (the software to accompany this application note is available on SMSC's FTP server at 1-516-233-4272 or via the World Wide Web at <http://www.smisc.com/ftpdocs/chips.html>. Download the file, named "constest.zip" in the "appsoftware" directory). This software in conjunction with SMSC Evaluation Boards or customers motherboards will provide the user with a way to exercise the Consumer IR block. The final part of the application note will give a low level software outline of how to do Consumer IR transmits and receives. Future SMSC application notes will deal with the Consumer IR block at a higher software level.

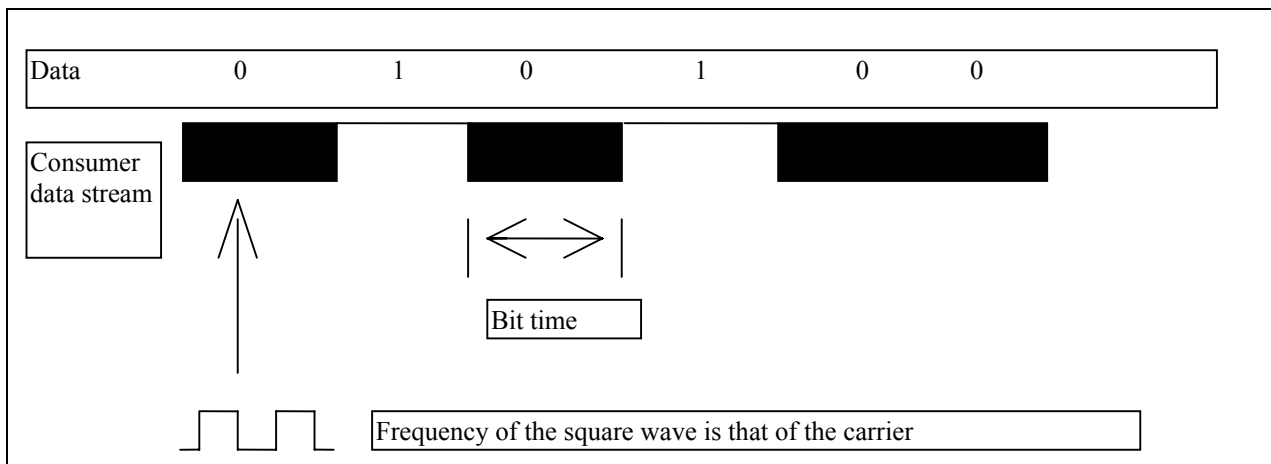


FIGURE 1 - STANDARD CONSUMER IR

Standard Consumer IR

Unlike FIR and SIR which have well defined protocols that can be adhered to by all manufacturers, Consumer IR protocols suffer from a lack of consistency and vary from manufacturer to manufacturer. However at the lowest level, most Consumer protocols can be represented in the same way. A bit rate is defined, a carrier rate is defined, a low level '0' is then represented by a bit rate time with the carrier active, a low level '1' is defined by a bit rate time with no activity on the line.

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To do a consumer transmit:

- 1) Consumer mode is selected
- 2) The desired carrier rate and bit rate are programmed
- 3) Data is placed in the FIFO
- 4) Transmit is enabled

Consumer data will be transmitted until the FIFO goes empty.

Several more options must be considered when doing a standard consumer receive. The first is carrier frequency sensitivity. Because the received carrier frequency may not exactly match the programmed carrier frequency, varying carrier frequency sensitivities (10, 20 or 40%) can be selected. If a carrier frequency outside the range is detected the frame abort bit is set. Another option that must be set is the sync bit. This option enables the bit sync logic on the receiver.

To do the Consumer receive:

- 1) Consumer mode is selected
- 2) The desired carrier rate and bit rate are programmed
- 3) Carrier sensitivity and sync are selected
- 4) The receiver should be enabled

Appropriate consumer data will be received until the FIFO goes full. Software outlines of potential receive and transmit routines can be found at the end of this application note in the brute force transfer section.

NEC Framing

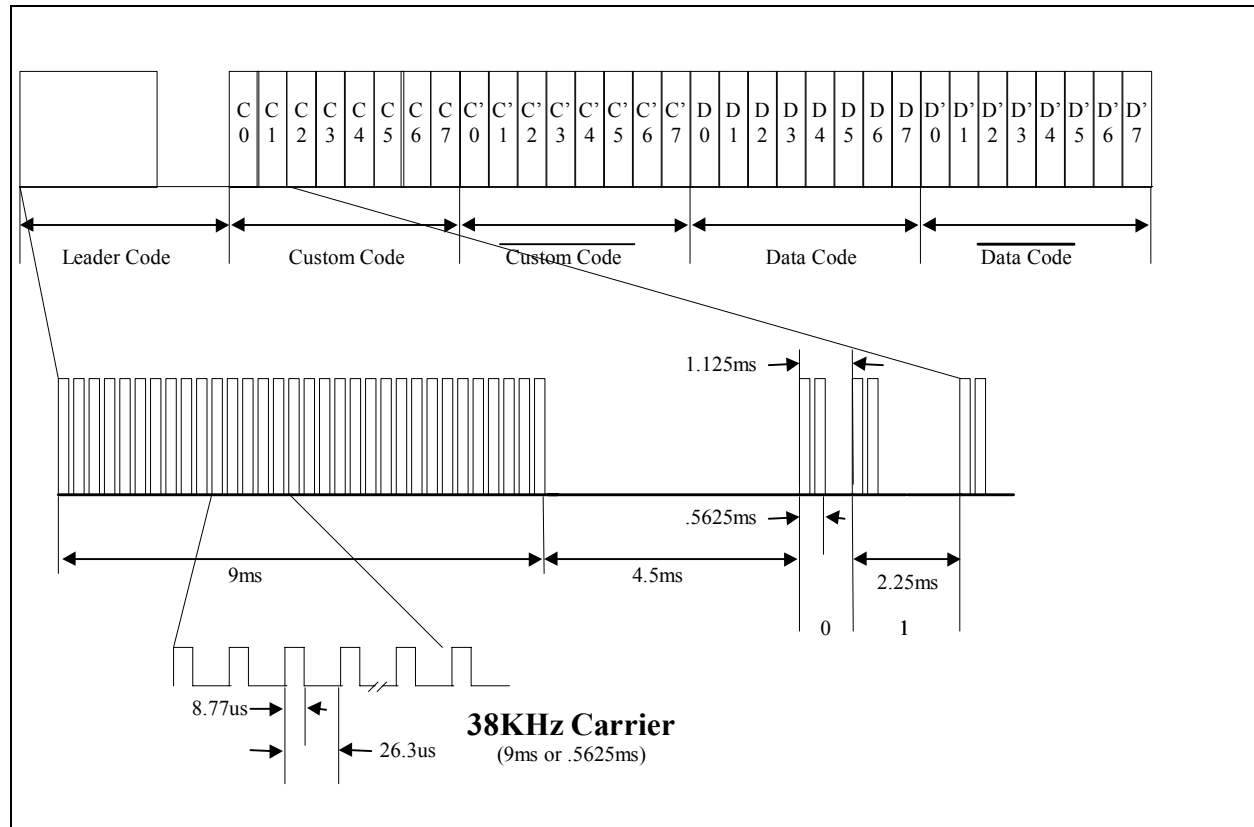


FIGURE 2 - NEC FRAMING (FDC37B77x ONLY)

The consumer block of the FDC37B77x supports NEC framing in receive mode only. The NEC framing Data Link Protocol consists of a leader code, an 8bit custom code, an 8 bit custom code bar, and 8 bit data code, and an 8 bit data code bar. The custom code can represent the specific device (TV, VCR) and the data code can represent the specific key code. The 'bit' rate is 1.88kHz and the carrier rate is 38kHz. The leader code is 9ms (16 bits) of '0' and 4.5ms (8 bits) of '1'. The data is a pulse position modulation scheme. An NEC '0' is represented by an '0' followed by a single '1'. An NEC '1' is represented by a '0' followed by a three '1's.

The FDC37B77x has added consumer registers and bits to accommodate NEC framing. When the 'framing' bit is set NEC frames will be looked for. Depending on the 'wake' bit, the custom and data code received, and the state of the 'no care custom code' (NCCC) and 'no care data code' (NCDC) bits, one of three things can happen:

- 1) A PME wakeup event will occur (No data is placed in the FIFO in this case, only wakeup occurs as the chip was 'asleep').
- 2) Decoded NEC data is placed in the RX FIFO.
- 3) Nothing will happen because the correct NEC frame was not decoded.

Table 1 shows the combination of possibilities and the resulting action. It is actual test data that was taken for device evaluation, so specific register settings and universal remote control codes are given.

Table 1 - Consumer IR Behavior Due to Various Receive Data and Register Settings

WAKE BIT	NCCC BIT	NCDC BIT	CUSTOM CODE REG	DATA CODE REGISTER	NEC CODE SENT BY UNIVERSAL REMOTE CONTROL	RESULTS
0	1	1	04 FB	AA	04 FB 11	04 FB 11 placed in FIFO
0	1	1	03 FB	AA	04 FB 11	04 FB 11 placed in FIFO
0	0	1	04 FB	AA	04 FB 11	11 placed in the FIFO
0	0	1	03 FB	AA	04 FB 11	No receive of data
1	1	1	04 FB	AA	04 FB 11	PME consumer status bit set
1	1	1	03 FB	AA	04 FB 11	PME consumer status bit set
1	0	1	04 FB	AA	04 FB 11	PME consumer status bit set
1	0	1	03 FB	AA	04 FB 11	PME consumer status bit not set
1	0	0	04 FB	11	04 FB 11	PME consumer status bit set
1	0	0	04 FB	11	04 FB 12	PME consumer status bit not set

Note: The frame bit was set for all above transactions. If configuration registers are set properly, the PME consumer status bit will be reflected on the PME output pin.

How to Use SMSC's In-House Consumer Software

'Low-level' in-house software was written to debug our IRCC and CIRCC cores. The name of the program is 'CONSTEST'. This program supports all SMSC devices with IRCC and CIRCC blocks, and does FIR and Consumer transfers. This manual will focus on the consumer aspects of the program. The program is meant to be used with SMSC Evaluation Boards, and should work with SMSC parts mounted on motherboards as well. The test requires two nodes (one for transmit, one for receive) connected by a cable which carries the Consumer signals (this cable is a simple two wire cable with 4 pin headers on each end, pins 1, 3 are cross wired). An optional laplink cable should connect COM1 of both nodes to perform handshaking if loop testing is desired. An alternate way of testing Consumer receive is to do a single node test using a demo card with a Temec module as the receiver and a universal remote control (URC) as the transmitter.

Hardware Setup

For a two node or one node Evaluation Board setup, consult table 2. It shows what jumpers need to be set on the boards and which header to use for the consumer cable (2 node test) or Temec module (single node test with URC). It also shows which output mux setting to use (selected within the program) that corresponds with the given header. Also, some parts require a configuration program to be run before the Consumer demo program is run.

Table 2- Evaluation Board Hardware/Software Setup

PART	IR HEADER TO CONNECT CABLE	CONFIG PROGRAM NEEDED BEFORE TEST IS RUN?	OUTPUT MUX SETTING	BOARD JUMPERS ASSOCIATED WITH IR HEADER
93xFR	JP67	NO	IR	JP95 1-2,3-4
67x	JP34	NO	IR	None
61x(60x)	Primary IR J7		IR	None
669FR	Primary IR	NO	COM	JP21,JP22 2-3
769LV	Primary IR	YES, CRE52.exe for 3 volt operation, load lv3v for 5 volt operation, load lv5v	COM	JP3 1-2 JP2 1-2
CAM35C44	Primary IR J8	NO	IR	JMP2 1-2,3-4
FDC37B77x	J8	NO	IR	None
FDC37C95x (rev a board)	J44 (note-pin1 of cable to pin 4 of header!)	NO	IR	None
FDC37C95x (rev b board)	Primary FIR H17	NO Config program, but must run 'orionen.exe', which powers up 95x chip, before running 'constest.exe'	IR	None

Software

When constest.exe is run, it does a search for SMSC devices and determines where the configuration space is located. The SMSC device may not be correctly identified, but this is not a problem. If, however, the error message 'failed to enter config' appears, there is a problem with the Evaluation board or system and it must be resolved before the user can continue.

Main Menu

Option 1- SCE register read/write

This is a register editor for the SCE block. Reads and writes can be done. The SCE block uses an addressing scheme in which registers are organized in blocks. Each page of the register editor corresponds to an SCE register block. The page up and page down keys move the user to different blocks, and 'f5' writes the registers. The user does not need to use this option, but it is useful for debug. One word of caution, doing a TX or RX in another part of the program can reset or rewrite certain registers. This can cause some confusion if the registers are interrogated after they are manually written and then a transfer is done.

Option 2- Chip-level options

This option lets the user change parameters within the configuration space of the chip. These include the base address of the SCE block (default 0x300), base address of UART2 (default 0x2f8), the interrupt (default 3), and the DMA channel (default is 3). If these values do not conflict with resources already allocated on the motherboard, the user does not need to use this option. (This option does not work on the 37c669FR and the 769FR).

Option 3- SCE-level options

These options allow you to change parameters that affect the transfer. Below is a partial list of options. Options not listed are not applicable to Consumer transfers. This is different than menu option 1. Option 1 allows direct low level access to the registers, this option lets the user change specific parameters without worrying about which bits need to get set.

Table 3 - SCE Level Options

KEY	FUNCTION	DESCRIPTION
F1	SCE mode	Select HDLC, 4ppm or Consumer. For this test select consumer.
F2	TX polarity	Self-explanatory
F3	RX polarity	Self-explanatory
F4	Output mux	Many of our chips have multiple pins where the TX and RX data can be muxed to. This option selects which pins are selected.
F8	Carrier range	Select 10, 20 or 40%. In consumer receive mode selects the allowable deviation in the received carrier frequency. Set to 40% when using a real remote.
F7	Carrier off	For TX and RX determines if the bit time representing data '0's will be a static low level, or will be a square wave at the selected carrier rate. One is always a static level.
F9	IR carrier rate	Self-explanatory
F10	IR bit rate	Self-explanatory
F5	FIFO threshold	For 'brute force' transfers, the FIFO threshold determines when the SCE will start transmitting data (when the host places FIFO threshold number of bytes in the FIFO, the SCE will start Txing data).
SF4	Max poll multiplier	This controls software time-outs. It is useful for migrating to machines of different speeds.
B	Frame	Determines if NEC framing and protocol will be used in receive mode. The wake, NCCC, NCDC bits are only used if frame is enabled.
E	Wake bit	If the wake bit is set, and the 'correct' NEC frame is received, the Consumer PME wakeup event occurs. If the wake bit is not set, and the 'correct' NEC frame is received, the appropriate parts of the NEC frame are placed in the FIFO.
C	NCCC	No care custom code bit. If set to 'care', the custom code and custom code bar received in the NEC frame are compared to the programmed value of the custom code registers. A match is necessary to trigger the action selected by the wake bit. No match is necessary when the NCCC bit is set to 'don't care'.
D	NCDC	No care data code bit. If set to 'care', the data code received in the NEC frame is compared to the programmed value of the data code registers. A code match is necessary to trigger a wake up event.. No match is necessary when the NCDC bit is set to 'don't care'.
F	Custom code 1	This is the compare value for the received NEC custom code (first 8 bits).
G	Custom code 2	This is the compare value for the received NEC custom code bar (second 8 bits).
H	Data code	This is the compare value for the received NEC data code.
F6	Sync bit	For consumer receive, when the sync bit is on, the rx bit rate clock synchronization mechanism is enabled. When using a URC, enable sync.
I	Reset PME	Resets the PME registers in config and sets them up for a consumer wakeup event.
PGUP	TX delay	For some of our newer parts (core 2.0 SCE blocks including the FDC37C769, CAM35C44, and FDC37B77x), this programmed delay will occur between when the TX is enabled, and when the SCE actually starts transmitting data.

Option 4 - Transfers

Selection of this option brings up a sub-menu. For consumer operation, brute force transfers should be selected.

Brute Force Test Page

'Brute force' transfers mean that the host SCE interface will be done by a simple poll of the SCE FIFO status bits. For a TX, data is written to the FIFO, as long as the FIFO full bit is not active. For an RX, data is removed from the FIFO as long as the FIFO empty bit is not set.

Table 4 shows a description of the test options:

Table 4 - Brute Force Test Page Options

KEY	FUNCTION	DESCRIPTION
1	Single TX	Do a single transmit
2	Single RX	Do a single receive
3	Loop TX	Loop on transmit
4	Loop RX	Loop on receive
6	Buffer size	Sets the size of the transmit and receive buffers.
7	Data type	Selects the data for the buffer. In TX mode, if NEC1 or NEC2 is selected, a NEC frame will be simulated with the specified custom and data code. NEC framing can then be tested on the receiver.
8	View RX buffer	View RX buffer
9	View TX buffer	View TX buffer
A	Bit stuff adjust	When highlighted ("on"), will set the first and last byte of the data buffer to 'aa'. Present testing should be done with the bit stuff adjust off, which can be done by changing the buffer size.
F2	SCE options	Adjust the SCE options. This brings up the same menu as 'option3' in the main menu.
F	FIFO threshold	Adjust FIFO threshold.
F3,F4	PARTNER	When loop testing is done, a hardware handshake between the two nodes through the COM1 ports and a laplink cable is necessary. Set this to 'another node' when this is done. If single transfer testing is done or single node receive testing is done with a URC, set this to 'RAM mirror' (no handshaking).

Two Node Testing in Standard Consumer Mode

This test will show that the system and both nodes are working properly in Standard Consumer mode. The user will be able to scope the TX consumer data and observe the protocol.

1. Setup two nodes and attach the consumer cable to the appropriate IR header (see table 2). If you have a laplink cable, attach the laplink cable to the COM1 port of both nodes. Make sure the keyboards of both nodes are close enough so that they can be operated at the same time.
2. On both nodes, run the program (constest.exe, part of constest.zip), hit the space bar, select transfers (4), select brute force (1), select SCE options (F2). Consult the setup table, and set the output mux bit appropriately for the part being tested (F4) . Hit escape. Turn off the handshaking by hitting F3 and then F4 until 'RAM mirror' is selected for both the TX and RX partners.
3. If you have a scope, put your transmit node in a TX loop and observe the TX data on pin 3 of the IR header. To put it in a loop, hit 3, return. The test can be terminated by hitting the space bar twice. Do not go further if you can not observe the TX data.
4. Do a single node to node transfer. On the RX node hit '2', hit '1' on the TX node. Without the handshaking enabled, these keys must be hit in order and very close together in time. Both nodes should say pass.
5. Do a node to node loop test. Enable handshaking by hitting F3, F4 until 'another node' is selected. On the RX node hit '4', on the TX node hit '3'. Then hit return on both nodes. Both nodes should be looping and passing. Hit the space bar twice on both nodes to terminate test (it is advantageous to hit the spacebar on the receive node first).

Two Node Testing in NEC Consumer Mode (FDC37B77x Only)

This test will show that the system and both nodes are working properly in the newer, NEC Consumer mode. The user, will be able to scope the TX consumer data and observe the NEC protocol.

1. Follow steps 1 and 2 from above.

2. On the transmit node select NEC transmit by hitting '7' and then selecting F3 or F4. Even though the transmitter is a standard Consumer node, the data has been selected such that the NEC framing is adhered to.
3. If you have a scope, put your transmit node in a TX loop and observe the TX data on pin 3 of the IR header. To put it in a loop, hit 3, return. The test can be terminated by hitting the space bar twice. Do not go further if you can not observe the TX data. Note that transmit data looks like an NEC frame. The leader should be easily identified (9ms of carrier followed by 4.5 ms of DC).
4. On the RX side first set the receive buffer to 3 bytes (hit '6', then 3, return). This is all that is needed because after an NEC receive only 3 bytes are placed in the FIFO (Custom code, custom code bar, and data code). Also select SCE options (F2), turn the frame bit on (B), turn the NCCC (C) and NCDC (D) bits to don't care. Hit escape.
5. Do a single node to node transfer. On the RX node hit '2', hit '1' on the TX node. Without the handshaking enabled, these keys must be hit in order and very close together in time. The TX node should say pass. The receive node should only say 'data error'. This is good. View the receive buffer by hitting '9'. Note that the received data matches the transmitted simulated NEC data. Hit escape. To eliminate the data error, select data type ('7') and then load from read buffer ('9'). Repeat the transfer. Both nodes should now say pass.
6. Do a node to node loop test. On both nodes enable handshaking by hitting F3, F4 until 'another node' is selected. On the RX node hit '4', on the TX node hit '3'. Both nodes should be looping and passing.

Note that all three of the bytes of the NEC frame went to the FIFO. This is because the NCCC bit was set for don't care, so that all valid NEC frames are received. The user can play with the logic by setting the NCCC bit to care and observing that data reception only occurs when the received custom code and custom code bar matches the custom code and custom code bar registers. When a valid custom code is received (when NCCC is '0'), only the data code makes it to the FIFO.

Single Node Testing With a Temec Module and a Universal Remote Control, Using the NEC Consumer Mode

This test will show that Universal Remote Controls, and the combination of a FDC37B77x and a Temec module, work properly. Other IR modules such as HP and Sharp may be used, but SMSC provides Temec modules as part of the evaluation kit, so Temec is referenced by name in these descriptions.

1. Attach the Temec module to IR header J8 of the FDC37B77x board.
2. Program your Universal Remote for an NEC TV compatible format.
3. Run the program, hit the space bar, select transfers (4), select brute force (1), and select SCE options (F2).
4. Turn on the frame bit (B), turn the NCCC (C) and NCDC (D) bits to don't care, and hit escape.
5. If you have a scope, observe the RX pin (pin 1 of the IR header). Put the remote close (approx 6 inches) to the Temec module and hit a key on the remote. The data should look like NEC data, and the carrier should be the correct frequency (38kHz). This verifies that the URC is properly programmed for NEC data.
6. Change the receive buffer size to 3 (hit '6','3', ret). Hit 2 for receive and then very quickly hit a key on the remote. A data error will occur (not a real data error). Observe the received data. It is a NEC code.
7. As above, the user can play with the NCCC bit and the custom code and custom code bar register to observe the results.

Compatibility testing has been done with the following URC's: Radio shack, One for all, Sole control, RCA, and Sony. If a user finds a URC that does not work with the FDC37B77x, please report to SMSC Applications engineering or your local sales office.

For reference, some NEC key codes: power 04 FB 08, volume up 04 FB 02, volume down 04 FB 03, key 1 04 FB 11, key 2 04 FB 12

Generate a Wakeup Event With a Universal Remote Control

This test demonstrates the low power wake up ability of the FDC37B77x from NEC Consumer frames that the FDC37B77x is capable of.

1. Get the FDC37B77x working with the URC and receiving frames as described above.
2. Put the scope probe on TP5 of the FDC37B77x. This is the PME output pin.
3. Set up the FDC37B77x to look for a specific key code. Go to the SCE option page (F2). Enable the frame bit (b), change the NCCC bit (c) to care, change the NCDC (d) bit to care, set the PME wake bit (e) to PME wake, and make sure the custom code, custom code bar, and data registers are set to 04 4b 12 (this represents a hit of key 2). Now hit '1'. This goes into config and enables Consumer PME wake events. Hit escape.
4. Observe that the PME pin is high (inactive). Enable the Consumer receiver by doing a receive (hit '2'). The receive will fail because no data was received, but the consumer block still has the receiver active and is waiting for a specific NEC code.
5. Hit any key on the URC except key 2. The PME pin should remain high (inactive). When the proper key is hit (key 2), the PME pin will go low (active).
6. Re-enable the wakeup event by going to the SCE options page (F2), and hitting '1'.

Software Outline

Below are summaries the brute force TX and receive sections of the software. They can be used to get an idea of the way the Consumer block can be programmed. There are many ways to do Consumer transfers and this is just one of them. Also below is a description of how the registers are organized and a summary of the SCE initialization procedure.

Registers

For a complete description of the CIRCC block, consult the CIRCC data sheet, which can be found on SMSC web site at www.smisc.com. Below is a brief description of how the registers are organized within the CIRCC block.

The SCE contains many registers. The physical address space is only 8 bytes wide, so the registers are grouped into 5 blocks, with a master control register that selects the block.

For example, bits d2, d1, d0 of the Master control block provide the block select.

To read the CHIP ID register (located in block 3, offset 2), the lower bits of the Master control block (offset 7) should be written to 03, and then the chip ID register at the base address of the SCE block + 2 can be read. Assume that the base address of SCE block is at 0x200. Execute the following pseudo code to read the chip ID register:

```
IN SCE7 (0x207)          ;Do a read/modify/write to the master control register so that D0-
                          D3 ;point to block 3
OUT SCE7(0x207),
DDDDD011
IN SCE2 (0x202)          ;This is the read of the chip ID register
```

Throughout the rest of this software summary, SCE registers will be identified by their block number and offset:

BXPY: BX is block number, PY is the offset. Using this example, the chip ID register is block 3 offset 2, so it would be known as **B3P2**. Note that BXP7 is the Master Block Control register, and thus no block number is required.

SCE Initialization Procedure

Both the TX and RX routines use an SCE-register_set routine. There are many registers that need to be set up before a transfer can occur. Below is a summary of these registers. Also included are some values that can be used for a demo.

Table 5 - Suggested Register Values for CIRCC Demo

REGISTER NAME, REGISTER ID	VALUE	MEANING
SCE config reg A B1P0	0x30	TX, RX polarity high, half duplex off, Consumer mode
SCE config reg B B1P1	0x40	Set output mux bit to IR output
FIFO control register B1P2	0x01	Set FIFO thresh to 1
Consumer cont register B2P0	0x82	Carrier on, sync on, carrier range 40%, frame off (no NEC)
Consumer carrier rate B2P1	0x29	Carrier is 38kHz
Consumer bit rate B2P2	0x37	Bit rate is 1.88 kHz

Brute Force Transfers

A 'brute force' transfer is the simplest method for interfacing to the SCE FIFO. The bus status register contains 'FIFO not empty' and 'FIFO full' bits. During a transmit, when the host wants to place data in the FIFO, it just polls the 'FIFO full' bit; if the FIFO is not full, the host can place a single byte of data in the FIFO. For RX, the host can pull data from the FIFO so long as the FIFO is not empty.

Brute Force TX

```

out BXP7, 70h          ;reset SCE
out BXP7, 20h

call set SCE options   ;Load the various SCE options by writing many different registers.
                        ;These options and register are described above.

Out B4P3, B4P4         ;Load the desired TX buffer size into the TX data size registers

out BXP7, 20h          ;Enable interrupts
out BOP2, f0h

out BOP5, 40h          ;enable SCE TX

for I = 1 to BUFFER_SIZE_TX
    poll bit 6 of BOP6 and wait for 0,    ; this is bit 6 of the XXX register, it is the FIFO full bit. If the FIFO is
    if not 'FIFO not empty' error        ; not full, write data to the FIFO. If it is full, keep polling the bit.

        out BOP0, TXBUFFER [I]
next I

out BOP4, 02h          ; set data done bit in LCRA

poll bit 6 of BOP1 and wait for 1,      ;if not 'No end of message' error
out BOP3, 00h          ;Check line status registers for errors (Error are not really significant in
                        TX mode

in BOP3
if bit 7 = 1 'underrun error'
if bit 6 = 1 'overrun error'
if bit 5 = 1 'Frame error'
if bit 4 = 1 'Size error'
if bit 3 = 1 'CRC error'
if bit 2 = 1 'Frame abort error'

```

Brute Force RX

```
out BXP7, 70h          ;Reset SCE
out BXP7, 20h

call set SCE options   ;Load the various SCE options by writing many different registers.
                        ;These options and register are described above.
Out B4P3, B4P4         ;Load the desired RX buffer size into the RX data size registers

out BXP7, 20h          ;Enable interrupts
out BOP2, f0h

out BOP5, 80h          ;enable SCE RX

for I = 0 to BUFFER_SIZE_RX
  poll bit 7 of BOP6 and wait for 1, ; this is bit 7 of the XXX register, it is the FIFO empty bit. If the FIFO
  if not 'FIFO always empty' error   ; is not empty, take a single byte of data from it. If it is empty, keep
                                      ; polling the bit.
      in BOPO, RXBUFFER[I]
next I

out BOP3, 00h          ; Check line status registers for errors
in BOP3

if bit 7 = 1 'underrun error'
if bit 6 = 1 'overrun error'
if bit 5 = 1 'Frame error'
if bit 4 = 1 'Size error'
if bit 3 = 1 'CRC error'
if bit 2 = 1 'Frame abort error'

Check RX buffer against TX buffer
```



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