APPLICATION NOTE 7.9
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MII Management
Software Implementation for MII Compliant PHYs

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This Application Note provides the software developer with the necessary understanding to write software that configures MII compliant PHYs attached to SMSC's FEAST (LAN91C100XX) or EPIC (LAN83C1XX) family of devices. While general and attempting to be self-contained, focus is primarily on the SMSC devices and reference designs. The developer should refer to additional documentation, listed in the appendix, in order to get in depth knowledge of the MII management standard.

MII Management Interface Overview

The MII interface consists of a pair of signals that physically transport the management information across the MII, a frame format and a protocol specification for exchanging management frames, and a register set that can be read and written using these frames. The register definition (in the PHY) specifies a basic register set with an extension mechanism.

MII management refers to the ability of a management entity (S/W driver, setup utility, etc.) to "talk" to a PHY via the MII serial management interface for the purpose of displaying, selecting and/or controlling different PHY options. In order to do this the management entity manipulates a Station Management entity (STA) as a vehicle to drive the MII management serial interface. In the case of SMSC applications, the STA is located in the MAC controller (FEAST or EPIC). By manipulating the MAC's registers, MII management frames are generated on the management interface for reading or writing information from the PHY registers.

The following sections will provide a description of the electrical interface, management frame structure, and register map for both the PHY and MII-relevant part of MAC devices.

MII Management Electrical Interface

The MAC and the PHY communicate via the two-wire MII Management serial Interface. The signals are:

MDIO: Management Data input/output. Bidirectional signal between MAC and PHY that carries management data. All control and status information sent over this pin is driven and sampled synchronously to the rising edge of the MDC signal.

MDC: Management Data clock. Sourced by the MAC as a timing reference for transfer of information on the MDIO signal. MDC is a periodic signal with no maximum high or low times. The minimum high and low times should be 160 ns each and the minimum period of the signal should be 400 ns. These values are regardless of the nominal period of the TX and RX clocks (Ethernet data transfer clocks)

Management Frame structure

Table 1 - Management Frames

	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
READ	1…1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
WRITE	1…1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

The table above shows the format for the read and write management frames. Each character represents one 'bit' on the MDIO line.

The fields are:

PRE: Preamble. 32 contiguous logic '1's sent by the MAC on MDIO along with 32 corresponding cycles on MDC. This provides synchronization for the PHY.

ST: Start of Frame. Indicated by a 01 pattern

OP: Operation code. Read = 10. Write = 01.

PHYAD: PHY address. Up to 32 PHYs can be connected to one MAC. This 5 bit field selects which PHY the frame is directed to.

REGAD: Register Address. This is a 5 bit field that selects which one of the 32 registers of the PHY this operation refers to.

TA: Turnaround. This is a two bit time spacing between the register address and the data field of a frame to avoid contention during a read transaction.

DATA: Data. These are the 16 bits of Data.

IDLE:Idle Condition, not actually part of the management frame. This is a high impedance state. Electrically, the PHY's pull-up resistor will pull the MDIO line to a logic one .

The PHY Address is usually hardwired through hardware pins of the PHY device. Check your hardware schematics for the PHY Address you are using.

MII Registers in the PHY

Table 2 - PHY Register Map

REGISTER ADDRESS	REGISTER NAME	BASIC / EXTENDED
0	Control	B
1	Status	B
2,3	PHY ID	E
4	Auto-Negotiation Advertisement	E
5	Auto-Negotiation Link Partner	E
6	Auto-Negotiation Expansion	E
7	Auto-Negotiation Next Page Transmit	E
8 .. 15	Reserved	E
16 .. 31	Vendor specific	E

The basic register set consists of two registers: Control and Status. All PHYs that provide an MII should incorporate these two registers. The other registers in the table are optional MII defined (2 through 7) or proprietary (16 through 32) extensions.

The next section provides a brief description of the registers using the following convention:

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

The box below each bit denotes *Type* and *Power Up / Reset default value*.
Types are:

R: Read Only
W: Write Only
RW: Read/Write
SC: Self clearing
LH: Latch high
LL: Latch low

0. Control Register

Reset	Loopback	Speed	Nway Enab.	PwrDwn	Isolate	Nway Rest.	Duplex
RW, SC. 0	RW. 0	RW. 1 Note 1	RW. 1 Note 2	RW. 0	RW. 1	RW. SC. 0	RW. 0 Note 3

Coll. Test.	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
RW. 0	RW	RW	RW	RW	RW	RW	RW

Reset:

A ‘1’ written to this bit will initiate a reset of the PHY. The bit is self-clearing, and the PHY will return a ‘1’ on reads to this bit until the reset is completed. Write transactions to this register may be ignored while the PHY is processing the reset. All PHY registers will be driven to their default states after a reset.

Loopback:

Writing a ‘1’ will put the PHY into loopback mode.

Speed (Speed Selection):

When Auto Negotiation is disabled this bit can be used to manually select the link speed. Writing a ‘1’ to this bit selects 100 Mbps, a ‘0’ selects 10 Mbps.

When Auto-Negotiation is enabled reading or writing this bit has no meaning/effect, unless he PHY only supports one speed in which case the bit will always reflect that value and will not changed upon a write operation.
Note 1: The default of this bit is ‘1’ unless the PHY only supports 10Mbps (reported in status register) in which case the default is ‘0’

Nway Enab (Auto-Negotiation Enable):

Auto-negotiation (NWAY) is on when this bit is ‘1’. In that case the contents of bits *Speed* and *Duplex* are ignored and the NWAY process determines the link configuration.
If the PHY does not support NWAY this bit should be read as zero.
Note 2: The default of this bit is ‘1’ unless the PHY does not support NWAY (reported in status register) in which case the default is ‘0’

PwrDwn (Power down):

Setting this bit to ‘1’ will put the PHY in Power Down mode. In this state the PHY will respond to management transactions.

Isolate:

Setting this bit will set the PHY to an isolated mode in which it will respond to MII management frames over the MII management interface but will ignore data on the MII data interface

Nway Rest (Auto-Negotiation Restart):

This bit will return 0 if the PHY does not support NWAY or if NWAY is disabled through the *Nway Enab* bit. If neither of the previous is true, setting this bit to ‘1’ restarts the NWAY process. This bit is self clearing and the PHY will return a ‘1’ until NWAY is initiated, writing a ‘0’ does not affect the NWAY process.

Duplex (Duplex mode):

When Auto Negotiation is disabled this bit can be used to manually select the link duplex state. Writing a ‘1’ to this bit selects full duplex while a ‘0’ selects half duplex.

When Auto-Negotiation is enabled reading or writing this bit has no effect, unless the PHY only supports one duplex mode in which case the bit will always reflect that value and will not change upon a write operation.
Note 3: The default of this bit is ‘0’ unless the PHY only supports full duplex (reported in status register) in which case the default is ‘1’

Coll. Test (Collision test):

Setting a ‘1’ allows for testing of the MII COL signal. ‘0’ allows normal operation.

Reserved:

Reserved for future standardization. Should be written as 0 and ignored when read.

1. Status Register

100BaseT4	100BaseXD	100BaseXH	10Mbps-D	10Mbps-H	Reserved	Reserved.	Reserved
RO	RO	RO	RO	RO	RO	RO	RO

Reserved	MFPre Sup.	Nway Comp	Rem.Fault	Nway Ability	Link Status	Jabber Det.	Extend Cap
RO	RO	RO	RO, LH	RO	RO, LL	RO, LH	RO

100BaseT4: ‘1’ Indicates 100Base-T4 capable PHY, ‘0’ not capable.

100BaseXD: ‘1’ Indicates 100Base-X full duplex capable PHY, ‘0’ not capable.

100BaseXH: ‘1’ Indicates 100Base-X half duplex capable PHY, ‘0’ not capable.

10Mbps-D: ‘1’ Indicates 10Mbps full duplex capable PHY, ‘0’ not capable.

10Mbps-H ‘1’ Indicates 10Mbps half duplex capable PHY, ‘0’ not capable.

Reserved: Reserved for future standardization. Should be ignored when read.

MFPre Sup: MF Preamble suppression ability. '1' indicates the PHY is able to receive management frames even if not preceded by a preamble. '0' when it is not able.

Nway Comp Auto-Negotiation Complete. When read as '1' indicate Nway has been completed and that contents in registers 4,5,6 and 7 are valid. '0' means Nway has not completed and contents in registers 4,5,6 and 7 are meaningless. The PHY returns zero if it lacks the ability to perform Nway or Nway is disabled.

Rem. fault: '1' Indicates a Remote Fault. Latches the '1' condition and is cleared by reading this register or reseting the PHY.

Nway Ability: Indicates the ability ('1') to perform NWAY or not ('0').

Link Status: A '1' indicates a valid Link and a '0' and invalid Link. The '0' condition is latched until this register is read.

Jabber Det: Jabber Detect. Jabber condition detected when '1' for 10Mbps. '1' latched until this register is read or the PHY is reset. Always '0' for 100Mbps

Extend. Cap:. Extended Capability register. '1' Indicates extended registers are implemented

2,3. PHY Identifier Registers

These two registers (offsets 2 and 3) provide a 32 bit value unique to a PHY. The information includes manufacturer identifier, model within the manufacturer and revision number. Refer to the spec of the PHY you are using for further information. If you have several designs using different PHYs which you want to support with the same software, and the different PHYs have different proprietary features, these registers can be read to determine which type of PHY this is.

4. Auto-Negotiation Advertisement Register

Next Page	Reserved	Rem. Fault	TA7	TA6	TA5	TA4	TA3
RW	R0	RW	RW	RW	RW	RW	RW

TA2	TA1	TA0	S4	S3	S2	S1	S0
RW	RW	RW	RW	RW	RW	RW	RW

This register controls the values transmitted by the PHY to the remote partner when advertising its abilities

Next Page: A '1' Indicates the PHY wishes to exchange Next Page information. Beyond the scope of this Application Note. See references 1 and 3 for more information

Reserved: Write as '0'. Ignored when Read

Rem. Fault: Remote Fault. When set, an advertisement frame will be sent with the corresponding bit set. This in turn will cause the PHY receiving it to set the Remote Fault bit in its Status register

TA 0..7: Technology Ability Field. This byte holds the current technologies supported by the auto-negotiation standard. Currently the bits assigned are:
TA0 10Base-T
TA1 10Base-T Full Duplex
TA2 100Base-TX
TA3 100Base-TX Full Duplex
TA4 100Base-T4
TA5 Reserved for future technology
TA6 Reserved for future technology

TA7 Reserved for future technology

The management entity sets the value of this field prior to autonegotiation.
'1' in TAn bit indicates that the mode of operation that corresponds to Tan will be acceptable to be auto-negotiated to. Only modes supported by the PHY can be set.

S 0 ..4: Selector Field Value. For SMSC current devices (802.3) S[4..0] = 00001.

5. Auto-Negotiation Link Partner Ability Register

Next Page	Ack	Rem. Fault	TA7	TA6	TA5	TA4	TA3
RW	R0	RW	RW	RW	RW	RW	RW

TA2	TA1	TA0	S4	S3	S2	S1	S0
RW	RW	RW	RW	RW	RW	RW	RW

The bit definitions are analogous to the Auto Negotiation Advertisement Register except for the following:

Ack: Acknowledge. It is used by the Auto-negotiation function to indicate that a device has successfully received its Link Partner's Link code Word.

The PHY may support additional pages of information and wish to exchange them with its link partner. This is beyond the scope of this Application Note. See references 1 and 3 for more information.

6. Auto-Negotiation Expansion Register and
7. Auto-Negotiation Next Page Transmit Register

These two registers are used for the Next Page Exchange which is beyond the scope of this App-Note.

8-15 Reserved Registers

These Registers are reserved for future standardization by 802.3.

16-31 Vendor specific registers

These registers are vendor specific. If implemented, refer to the spec of the PHY you are using for details. For example, some PHYs implement the capability of generating an interrupt upon Auto-Negotiation completion.

MII Interface Registers in SMSC's MACs

EPIC family (LAN83C17X)

The interface is located in the Ethernet Register Map area at offset 30h through 3Bh.

30h. MMCTL (MII Management Interface Control Register)

Un	Un	Un	Un	Un	Un	Un	Un	Un	Un	Un	Un	Un	Un	Un	Un
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Un	Un	PA	PA	PA	PA	PA	RA	RA	RA	RA	RA	Res	Un	W	R
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Un: Unused
PA: (RW) PHY address. Bit 13 is MSB.
RA: (RW) Register address. Bit 8 is MSB.
Res: (R) Responder. A '1' will be returned during a read operation if the PHY drove a '0' following the 'Z' state in the TA field of the management frame. This bit can be used to determine if a PHY responded to a Read operation. This bit is self-clearing after the register is read.
W: (W) Write. Set to '1' to initiate MII management write cycle. Self-clearing.
R: (W) Read. Set to '1' to initiate MII management read cycle. Self-clearing.

34h. MMDATA (MII Management Interface Data)

Un	Un	Un	Un	Un	Un	Un	Un	Un	Un	Un	Un	Un	Un	Un	Un
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Un: Unused
D15..0: (RW) The Data in the MII management frame is a reflection of these bits for both read and write operations.

38h. MIICFG (MII Configuration)

Un	Un	Un	Un	Un	Un	Un	Un	Un	Un	Un	Un	Un	Un	Un	Un
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Un	Un	Un	Un	Un	Un	Un	Un	ADi	ADa	ACS	Esm	PP	694l	694	sme
0	0	0	0	0	0	0	0	0	0	0	1	X	X	0	0

All bits are RW except for PP and 694l, which are Read only.

Un: Unused

ADi: Alternate Direction. When set, and if serial management is disabled, the value in *ADa* is input from the MDIO pin

ADa: Alternate data. Reading this bit returns the value of MDIO. Writing it drives MDIO, if the serial management interface is disabled and *ADi* is set.

ACS: Alternate Clock source. When the serial management interface is disabled this bit is multiplexed to the MII management clock pin. A '1' drives the clock high.

Esm: Enable serial Management. If set the serial management is enabled. If cleared, the MDIO and MDC pins can be commanded by using the ADi, ADa and ACS bits.

PP: Phy Present. '1' indicates a PHY is present. Read only.

694l: Read only and returns the value id the 694LNK pin on the LAN83C17X.

694: Drives the EN694 pin of the LAN83C17X.

sme: When set, the MII interface functions serially as a 7-wire interface for connection of a 10 Mbps serial PHY device. When cleared, the MII interface operates as defined by the 802.3u standard.

FEAST family (LAN91C100XX)

Bank 1. Configuration Register

When *MIISel* (bit 15) = '1' FEAST uses its MII interface. If this bit is 0 serial interface for connection of a 10 Mbps PHY interface is used and not the MII.

Bank 3. Offset 08h. MGMT

FLTST	MSKCRS100						
0	0	1	1	0	0	1	1

				MDOE	MCLK	MDI	MDO
0	0	1	1	0	0	MDI Pin	0

FLTST: Not used for MII Management.
MSKCRS100: Not used for MII Management.
MDOE: MII management Output enable. If '1' MDIO is driven, if '0' MDIO is tristated.
MCLK: MII Management Clock. This bit drives the MDCLK (MDC) pin.
MDI: MII Management Input. Reads the value of MDIO.
MDO: MII Management Output. This value drives MDIO if MDOE is '1'.

Sample algorithms. Configuring an MII PHY in different modes

Writing a PHY register using the MACs register interface

EPIC (LAN83C17X)

EPIC has the capability of using the same set of chip pins to drive an MII interface or a 7-wire interface to connect to a 10Mbps serial PHY device. It also allows manual manipulation of the MDI and MDC signals. In order to use the standard MII interface and enable the complete PHY addressing capabilities (as opposed to the manual mode), the configuration should be set to *MIICFG* = 00000010h (only Esm set. See MIICFG register description above for additional details)

To read or write a PHY register:

Write: Load D0-15 with the value to write to the PHY register in MMDATA. Load PA, RA and set W=1, R=0 in MMCTL.

Read: Load PA, RA and set W=0, R=1 in MMCTL. Read MMCTL and verify Res = 1 for valid read, if not retry the operation. Read PHY Register value in D0-15 from MMDATA. Refer to the device driver source code for examples.

FEAST (LAN91C100XX)

FEAST support is far less elaborate than the one present in EPIC. MII management frames have to be built bit by bit by manipulating the MDI, MDO, MDOE and MCLK bits. Following is 'C' language code that implements both Read and Write operations.

```
// TYPES

typedef unsigned char  uchar;

// DEFINES

#define MGMT           port+0x08      // FEAST Registers
#define BANKSEL        port+0x0E

#define MDO            0x01           // MII Resgiter bits
#define MDI            0x02
#define MCLK           0x04
#define MDOE           0x08
#define MALL           0x0F
#define OPWrite        0x01
#define OPRead         0x02

// GLOBAL VARIABLES

unsigned int   port=0x300;

// FUNCTIONS

void clkmdio(unsigned MGMTData)
{
  outword(MGMT, MGMTData);
  outword(MGMT, MGMTData | MCLK);
}

unsigned PHYAccess(uchar PHYAdd, uchar RegAdd, uchar OPCode, unsigned wData)
{
 // Local variables

 int i;
 unsigned MGMTval;

 // Filter unused bits from input variables.

 PHYAdd &= 0x1F;
 RegAdd &= 0x1F;
 OPCode &= 0x03;

 MGMTval = inword(MGMT) & (MALL ^ 0xFFFF);

 // Output Preamble (32 '1's)

 for (i=0;i<32;i++)
  clkmdio(MGMTval | MDOE | MDO);

 // Output Start of Frame ('01')

 for (i=0;i<2;i++)
  clkmdio(MGMTval | MDOE | i);

 // Output OPCode ('01' for write or '10' for Read)

 for (i=1;i>=0;i--)
  clkmdio(MGMTval | MDOE | ((OPCode>>i) & 0x01) );

 // Output PHY Address

 for (i=4;i>=0;i--)
  clkmdio(MGMTval | MDOE | ((PHYAdd>>i) & 0x01) );

 // Output Register Address

 for (i=4;i>=0;i--)
  clkmdio(MGMTval | MDOE | ((RegAdd>>i) & 0x01) );

 if (OPCode == OPRead)
 {
  // Read Operation

  // Implement Turnaround ('Z0')

  clkmdio(MGMTval);
```

```
// The following line is commented out since the National PHY has a bug which will cause a
// 1 bit miss-alignment if it is included. Please note that in order for the code to be
// fully MII Management compliant the line should be uncommented.

//  clkmdio(MGMTval | MDOE);  // COMMENT OUT FOR NS PHY (BUG), LEAVE FOR OTHER PHYs.

  // Read Data

  wData = 0;

  for (i=15;i>=0;i--)
  {
   clkmdio(MGMTval);
   wData |= (((inword(MGMT) & MDI) >> 1) << i);
  }

  return (wData);
 }
 else
 {
  // Write Operation

  // Implement Turnaround ('10')

  for (i=1;i>=0;i--)
   clkmdio(MGMTval | MDOE | ((2>>i) & 0x01));

  // Write Data

  for (i=15;i>=0;i--)
   clkmdio(MGMTval | MDOE | ((wData>>i) & 0x01));

  return (1);
 }
```

Setting the Link Configuration of an MII manageable PHY. Examples.

We recommend that all the procedures listed below should start with the following two step sequence, especially during initialization time:
- Reset PHY by writing 1000h to PHY register 0.
- Poll bit 15 (*Reset*) in PHY register 0 until it is 0 for the reset completion. Timeout and report failure if it takes longer than 0.5 seconds.

Static 10BaseT Half duplex configuration:

1. Write 0000h to PHY register 0.
2. Set the duplex configuration of the MAC accordingly.

Static 100BaseTX Full duplex configuration:

1. Write 2100h to PHY register 0.
2. Set the duplex configuration of the MAC accordingly.

Auto-negotiation

The idea of auto-negotiation is that the PHY devices of the two nodes connected ("link-partners") will exchange information through the network according to a specified electrical/logical protocol and agree to configure themselves to a certain configuration which both of them support providing the maximum performance available. The protocol involves several steps (i.e. advertising the PHY capabilities, negotiating the "common denominator"). The software intervention is usually limited to issuing the auto-negotiation start command and waiting for its completion. The standard provides mechanisms to restrict to a subset the PHY's capabilities that are advertised during auto-negotiation. A complete discussion of Auto-Negotiation is very complex and beyond the scope of this App Note. We present a simple case below.

1. Set *NWAY enab* = ‘1’ in PHY register 0.
2. Set PHY register 4 to the desired features to be advertised. If not changed, the default value of this register will use the corresponding bits of the PHY Status register, which represent the full capabilities of the device.
3. Set *NWAY Rest* =’1’ in register 0. This starts the NWAY process
4. Poll the *NWAY Complete* bit in register 1 until it is ‘1’ indicating completion.
5. If relevant (depends upon PHYs implementation of the bit), check the *Rem.Fault* bit in Register 1 and process fault accordingly if set.
6. The driver or utility should inquire the PHY to find out the mode of operation it is on upon NWAY completion (by reading registers 4 and/or 5) and set the corresponding MAC registers to matching values if necessary. We discuss these settings in the following section.

Setting the MAC to match the PHY’s configuration.

Once the link-partner PHYs have completed the auto-negotiation process, or manual configuration of a PHY has been selected, the MAC has to be set to match those capabilities.

<u>EPIC</u>

When using the MII interface, speed differences (10/100 Mbps) are automatically handled at the MII without need for any specific register settings in the MAC. For duplex mode however, the matching mode has to be selected in bits 1 and 2 of the Transmit Control Register.

Bits 21	00	01	10	11
Mode	Half duplex	Int. Loopback	Ext. Loopback	Full duplex

<u>FEAST</u>

Same as EPIC, when *MIISel* =’1’ (bit 15 in Bank 1) only the duplex mode of FEAST has to be selected to match the mode in use by the PHY. This selection is done using the *FDSE* bit in the *TCR* (offset 0 in Bank 0) where *FDSE = ‘1’* enables full duplex.

<u>One Example using a 10Mbps PHY and a 100Mps PHY together</u>

Early implementations of 10/100 Mbps boards such as SMSC’s LAN9000-EVB103 used two PHYs to provide both speeds functionality with FEAST.

LAN83C110 (“Bacon”) is an early 100Mbps only PHY that supports the MII interface for TX/RX but is not MII manageable (no MII management interface or registers). Bacon was used in conjunction with an LAN83C694 10Mpbs serial PHY to provide a 10/100 solution in this board.

Bacon’s duplex control is provided via hardware by the FDSE pin (41). A multiplexing mechanism is provided via Pin *CHK10* (40), which controls the output on *LINK* (77) using either the 100Base-TX link or the value on the *LLEDIN* (which should be tied to the Link output of the LAN83C694), to provide a unique link signal (with information on 10 or 100 Mbps link) to FEAST without using external logic.

The software for this kind of board manipulates many bits in the MAC to select the different modes of operation. In the case of EVB103: *MIISel, AUI, Full Step (*in *Configuration* register*)* and *FDSE (*in *TCR)* were used to provide this control. Refer to this board’s schematics and documentation for further details.

Appendix: References

1) IEEE 802.3u Supplements. (Specially Clauses 22 and 28).
2) Data Sheets of the SMSC MACs (91C100FD, 83C170, 83C175, etc)
3) Data Sheets of PHYs (i.e. QS6612, NS83840, ICS1890, LAN83C110)
4) Schematics and documentation for FEAST and EPIC evaluation boards.
5) SMSC Software drivers', FEASTPHY.EXE and ETX.EXE utilities documentation and source code.

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