DUAL FOOTPRINT CONFIGURATION FOR THE FDC37N958FR AND THE FDC37N972

OVERVIEW

- The SMSC FDC37N972 and the FDC37N958FR are 208-pin ISA Ultra I/O Controllers for mobile applications. These devices are pin-compatible with the following exceptions, which are the subject of this document.
- The FDC37N972 is a next generation version of the FDC37N958FR. Attention will be focused here on developing Intel PIIX4-compatible motherboard designs that can accommodate either device.
- Design considerations include pin configuration variations due to feature changes in the FDC37N972, as well as the effects of incorporating the FDC37N958FR which is a 5V controller in a 3.3V system designed for the FDC37N972.

PIN CONFIGURATION CHANGES

- Significant feature additions to the FDC37N972 include PCI Clock Run support; enhanced ACPI functionality, including VCC1-powered wake events on all GPIO pins; an ACPI-compliant Embedded Controller Interface, ACPI PM1 block, and dedicated SCI pins; and a 512k-byte Flash ROM interface that includes two new pins FA18 and nFCS.
- FDC37N958FR features that are not found in the FDC37N972 include ISA Parallel IRQs, Serial Port 2, and the FDC Media ID pins.
- The effects of these changes on the pin configurations of both the FDC37N972 and the FDC37N958FR are summarized below in Table 1. Figure 1 illustrates an arrangement of jumpers that can be used to implement a dual footprint configuration. Jumper programming for Figure 1 is described in Table 1. The pin numbers in Table 1 are for TQFP packages, only.

TABLE 1 - DUAL FOOTPRINT JUMPER CONFIGURATION

	TQFP PIN #	FDC37N958FR		FDC37N972		DESCRIPTION
		PIN NAME	JUMPER (NOTE 1)	PIN NAME	JUMPER (NOTE 1)	
1	19	MID_0	J1	FPD	J2	In the FDC37N972 the MID_0 pin is not supported and the FPD pin has moved.
2	20	GPIO16	J3	IRTX	J4	These pins have been moved to simplify internal power bussing.
3	21	FPD	J5	IRRX	J6	
4	29[2]	VCC2	J7	VCC1	J8	In the FDC37N972 pin 29 is changed to support the functions added to VCC1.
5	45	EMCLK	J9	GPIO20	J19	These pins have been moved to simplify internal power bussing.
6	46	EMDAT	J11	GPIO21	J12	
7	52	GPIO20	J13	EMCLK	J14	
8	53	GPIO21	J15	EMDAT	J16	
9	100	IRQ4	J17	nCLKRUN	J18	In the FDC37N972 parallel IRQ pins except for nIRQ8 and nSMI are not supported. In the FDC37N958FR the nCLKRUN pin is not supported.
10	102	OUT7	J19	nRESET_OUT	J20	These pins have been moved to simplify internal power bussing.
11	105	VCC1_PWRGD	J21	24MHz_OUT	J22	
12	106	nRESET_OUT	J23	nEC_SCI	J24	In the FDC37N958FR the nEC_SCI pin is not supported.
13	109	24MHz_OUT	J25	VCC1_PWRGD	J26	These pins have been moved to simplify internal power bussing.
14	144	GPIO13	-	FA18	-	In the FDC37N958FR the FA18 pin is not supported and GPIO13 is an alternate function[3].
15	184	GPIO0	-	nFCS	-	In the FDC37N958FR the nFCS pin is not supported and GPIO0 is an alternate function[4].
16	203	IRRX	J27	OUT7	J28	These pins have been moved to simplify internal power bussing. NOTE: nSMI, the alternate function of the OUT7 pin, is an open-drain output in the FDC37N972 and a push-pull output in the FDC37N958FR.
17	204	IRTX	J29	GPIO16	J30	
18	29[2], 143, 176	VCC1	J31	VCC1	J32	In the FDC37N972, VCC1 is 3.3V. In the FDC37N958FR, VCC1 is 5V. (see Section 0 3.3V/5V , below)
19	29[2], 83, 104, 120, 205	VCC2	J33	VCC2	J34	

NOTE 1: Jumpers listed in Table 1 refer to Figure 1. The jumpers per pin are mutually exclusive and depend on the selected device. To enable a pin function, short the jumper with a 0 ohm resistor.

NOTE 2: In the FDC37N972 this pin is switched from VCC2 to VCC1 (see Item #4 in Table 1).

NOTE 3: In dual footprint designs, a 256k byte FlashROM can be used for maximum backward compatibility. In dual footprint designs with a 512k byte FlashROM requirement, GPIO13 in the FDC37N958FR can be used to emulate FA18 in the FDC37N972. To do this, send an 8051 command to update GPIO13 when the HMEM register is written.

NOTE 4: In dual footprint designs, GPIO0 in the FDC37N958FR can be used to emulate the nFCS pin in the FDC37N972.

3.3V/5V SYSTEMS

- 3V logic families have the same I/O specifications as 5V TTL families but with a 3.3V VCC instead of 5V. But even though the interface specifications between these families are otherwise compatible, in some cases level shifters are required to prevent damage to specific 3.3V LVTTL inputs when using the FDC37N958FR - which is a 5V only device - in 3.3V PIIX4 systems that are designed for the FDC37N972.
- As an example, the PIIX4 SUSPEND power plane VCC (SUS) and the RTC power plane VCC (RTC) contain the real-time clock, CMOS RAM, and specific logic needed to resume the system from the suspend state. Inputs powered by these voltage planes do not support 5V input levels and must not exceed VCC (SUS) or VCC (RTC). The affected PIIX4 pins are shown in Table 2.

TABLE 2 - PIIX4 RTC AND SUSPEND POWER PLANES

POWER PLANE	DESCRIPTION	SIGNALS POWERED	VCC PINS	GND PINS
RTC	Contains the real-time clock and 256 bytes of battery-backed SRAM. The input signals attached to the RTC power plane DO NOT SUPPORT 5 VOLT INPUT LEVELS. These signals must not exceed VCC (RTC).	PWROK nRSMRST RTCX1, RTCX2	VCC (RTC)	VSS
SUSPEND	Contains the logic needed to resume from the Suspend-to-Disk and Suspend-to-RAM states. The input signals attached to the SUSPEND power plane DO NOT SUPPORT 5 VOLT INPUT LEVELS. These signals must not exceed VCC (SUS).	nBATLOW CONFIG[1:2] nEXTSMI GPI[1] nIRQ8 LID nRI nSMBALERT SMBCLK SSMMBDATA nPWRBTN nSUS[A:C] SUSCLK nSUS_STAT[1:2] nTEST	VCC (SUS)	VSS

Level shifters are absolutely required for FDC37N958FR-populated dual footprint designs when the PIIX4 VCC (RTC) and VCC (SUS) power planes are 3.3V.

Generally, it is recommended that level shifters like the QS3384 QuickSwitch bus switches from Quality Semiconductor be used in all FDC37N972 and FDC37N958FR dual footprint designs for any signals that drive the PIIX4 pins shown in Table 2. Typically, devices like the QS3384 do not need to be removed for 97X-populated designs because they do not affect the LVTTL interface and contribute negligible signal delays.

For specific application examples using the FDC37N958FR in 3.3V PIIX4 designs, consult SMSC Application Note 7.8 FDC37N958FR DESIGN GUIDE.

REFERENCES

- SMSC FDC37N972 DATA SHEET
- SMSC FDC37N958FR DATA SHEET
- SMSC APPLICATION NOTE 7.8 FDC37N958FR DESIGN GUIDE
- INTEL 82371AB PIIX4 PCI TO ISA/IDE XCELERATOR
- QUALITY SEMICONDUCTOR, INC., APPLICATION NOTE AN-11A BUS SWITCHES PROVIDE 5V AND 3V LOGIC CONVERSION WITH ZERO DELAY.

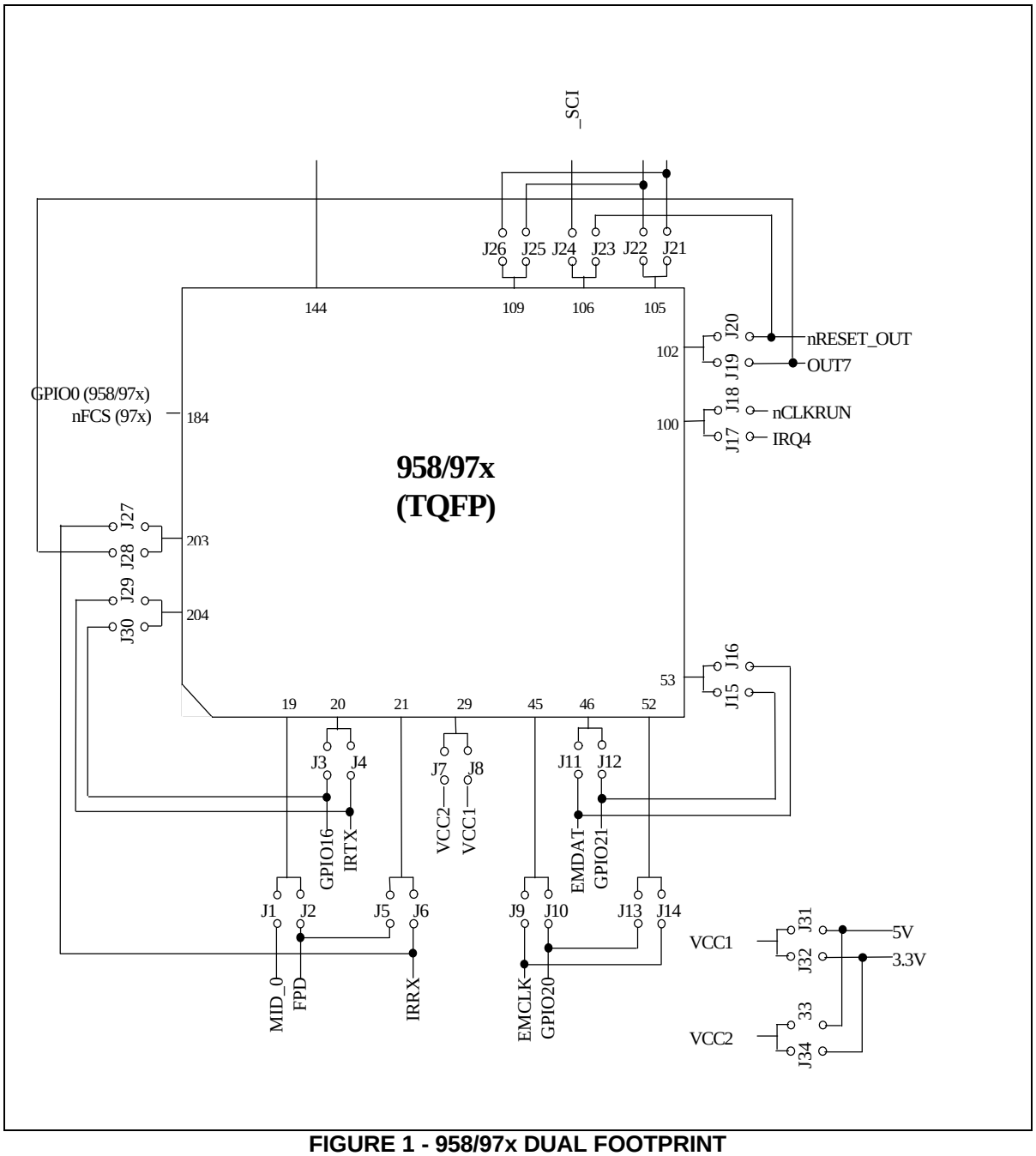

FIGURE 1 - 958/97x DUAL FOOTPRINT

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