



APPLICATION NOTE 8.10

LAN91C100FD Rev. B/LAN91C110 Rev. A Minimum SRAM Access Time Requirement and a List of Recommended SRAMs

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INTRODUCTION

The LAN91C100FD Rev. B/LAN91C110 Rev. A Ethernet Controllers utilize external SRAM to store and forward Ethernet packets to and from the Host. The LAN91C100FD Rev. B/LAN91C110 Rev. A were originally designed to work with SRAMs that are no longer widely available. Improvement in process technology and smaller geometries has resulted in faster access times. The latest generations of SRAMs benefiting from these advances have measured access time approaching 5ns. The LAN91C100FD Rev. B/LAN91C110 Rev. A cannot work with SRAM access time faster than 8ns. Access time faster than 8ns will result in data corruption.

Unfortunately, the designer cannot rely on published access times in choosing the SRAM for their application since there is no consistency in the guardband between different manufacturers. The differences between actual and published access time is not consistent. For example, a Cypress 25ns SRAM is actually faster than an Alliance or Hyundai 12ns SRAM.

To alleviate this situation, this Application Note provides a list of SRAMs that meet the access time requirement. Besides meeting the access time requirements, the SRAMs listed in Table 1 passed extensive functional testing and are guaranteed at all operating conditions.

Additionally, Table 2 is a list of SRAMs to avoid. These SRAMs failed in our testing and/or have access times with very small margin. Both lists include the rated and measured access times.

SMSC will update these lists periodically since the SRAM market is continually evolving.

Minimum Read Data Hold Time - t_{HOLD}

The LAN91C100FD Rev. B/LAN91C110 Rev. A latch the SRAM data during a read operation at the trailing edge of the address transition requiring a minimum hold time of 8ns (t_{HOLD}). As illustrated in Figure 1, Rd data1 is latched on the Addr1 to Addr2 transition. Rd data1 has to stay on the Bus for at least $t_{\text{HOLD}} = 8\text{ns}$, otherwise the data is corrupted. Since the control signal nOE remain active during successive read operations (becomes inactive with a write operation), the address transition will cause Rd data2 to appear on the Bus an access time later.

Therefore, the SRAM access time is the read data hold time. SRAMs with access time less than 8ns do not meet the minimum read data hold time.

Note: The SRAM data sheets usually specifies a data hold after address transition of 3ns, but our investigation shows the data is held until the valid next data. The SRAMs in the recommended list have this parameter in their data sheets, yet they passed all the testing.

SRAM Recommendations for LAN91C100FD Rev. B/LAN91C110 Rev. A Applications

Table 1 - SMSC recommends the Alliance and Hyundai 15ns, Hitachi 25ns, and Mosel Vitelic 35ns SRAMs for LAN91C100FD Rev. B/LAN91C110 Rev. A applications, based on measured access times and extensive RAM testing. The greater than 11ns access time provides an adequate hold time for the LAN91C100FD Rev. B/LAN91C110 Rev. A.

SRAMS RECOMMENDED FOR LAN91C100FD REV. B/LAN91C110 REV. A APPLICATIONS			
MANUFACTURER	PART NO.	ACCESS TIMES (NS)	
		DATA SHEET	MEASURED
Mosel Vitelic	V62C518256-35F	35	14
Mosel Vitelic	V62C518256L-25R	25	12
Alliance	AS7C256-15	15	12
Hyundai	HY638256-LJ 15	15	11
ISSI	IS61C3216-15T	15	10

Table 2 - This table lists SRAMs that will fail in LAN91C100FD Rev. B/LAN91C110 Rev. A applications. Although some of the SRAMs (like the Cypress 12ns & 25ns) passed all testing, the access time is too close to the 8ns limit.

SRAMS NOT RECOMMENDED FOR LAN91C100FD REV. B/LAN91C110 REV. A APPLICATIONS			
MANUFACTURER	PART NO.	ACCESS TIMES (NS)	
		DATA SHEET	MEASURED
Winbond	W24257AJ-12	12	6
Cypress	CY7C199-12VC	12	8
Cypress	CY7C199-15VC	15	5
Cypress	CY7C199-25VC	25	9
Cypress	CY7C199-35VC	35	6
Hitachi	HM62832-25	25	9
Galvantech	GVT72024A8TS-15	15	9
Toshiba	TC558128 BF T-15	15	7
ISSI	IS61C256AH-15J	15	7
Mosel Vitelic	V61C518256-12R	12	7
Mosel Vitelic	V61C518256-15R	15	7
IDT	IDT 71256 SA15Y	15	8

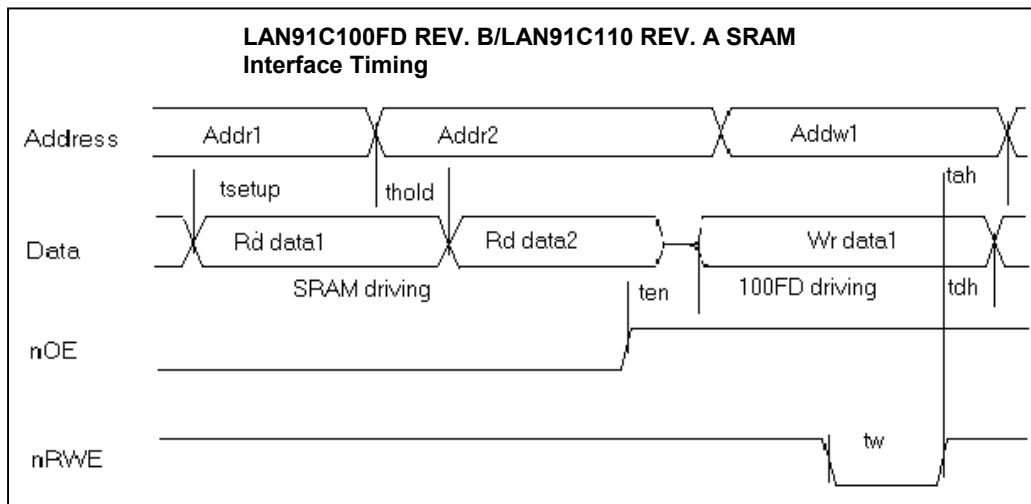


FIGURE 1

Table 3 - LAN91C100FD Rev. B/LAN91C110 Rev. A SRAM Interface Timing illustrating t_{hold} . Missing parameters are also included in the data sheet. One caution is t_{en} . Bus contention is possible whenever this value is less than the output disable time of the SRAM driver after nOE is deasserted. Preliminary t_{en} is 0ns, which will result in Bus contention. No detrimental effect was apparent due to the contention.

PARAMETER		MIN (NS)	MAX (NS)
Read data setup to address change	t_{setup}	5	
Read data hold after address invalid (Thold)	t_{hold}	8	
nRWE0-nRWE3 pulse width	t_w	18	
Write data hold after nRWE0-nRWE3	t_{ah}	6	
Write address hold after nRWE0-nRWE3	t_{dh}	0	
Data Bus driving after nOE deasserted**	t_{en}	0	

** Data is preliminary