

Migrating from LAN91C100FD (FEAST FD) to LAN91C110 (Reduced-Pin-Count FEAST FD) Software Modifications in Drivers & Utilities By Pankaj Gupta & Ronnie Kunin

Overview

The LAN91C110 MAC provides a subset of the pin functions of the regular FEAST FD. The supported features include an ISA bus for the host interface. The network physical layer interface is limited to the MII. The new controller provides the same set of control registers as provided by the regular FEAST FD. On account of this new reduced-pin-count chip, the software modifications detailed in this application note are required in the LAN9000 software drivers or utilities to support the LAN91C110 chip.

Revision Register

The chip ID and Revision register located in BANK 3 at IO SPACE address 0x0A reads back 90H indicating the chip ID is '9' and the revision is '0' For the LAN91C110.

From the software point of view, it is required to read the Chip ID and Revision Register in order to identify and be able to differentiate between the different chips of the LAN9000 family.

Media Independent Interface (MII)

The LAN91C110 supports only the MII interface for connection of PHYs. There is no support for legacy serial transceivers since the pins that offered that support in the previous LAN91C100FD have been removed in the 91C110. However, since the register set of the LAN91C110 is identical to that of the LAN91C100FD, it still has the bits that allow for selection of serial transceivers (i.e.: MIISelect, AUISelect) in the predecessor chip.

In order for any software to work properly with the LAN91C110 the MIISelect bit in Configuration Register (bit 0x8000 at IO Space offset 0x00) in BANK 1 should always be set to 1. If it is desired to forcefully select media types, the software should program the PHY chip accordingly through the MII interface. See Application Note 7.9 for details on how to implement this support.

Interrupt Pins (INTR 0)

The LAN91C110 has only one interrupt pin (INTR0). However, since the register set is the same as the LAN91C100FD, it still offers the choice of up to 4 interrupt pins (INTR0-3) by setting up the appropriate INT SEL 0-1 bits in Configuration Register at BANK 1.

| INT SEL 1 | INT SEL 0 | LAN91C100FD INTERRUPT PIN USED | LAN91C110 INTERRUPT PIN USED |
|-----------|-----------|-----------------------------------|---------------------------------|
| 0 | 0 | INTR0 | INTR0 |
| 0 | 1 | INTR1 | Illegal Setting |
| 1 | 0 | INTR2 | Illegal Setting |
| 1 | 1 | INTR3 | Illegal Setting |

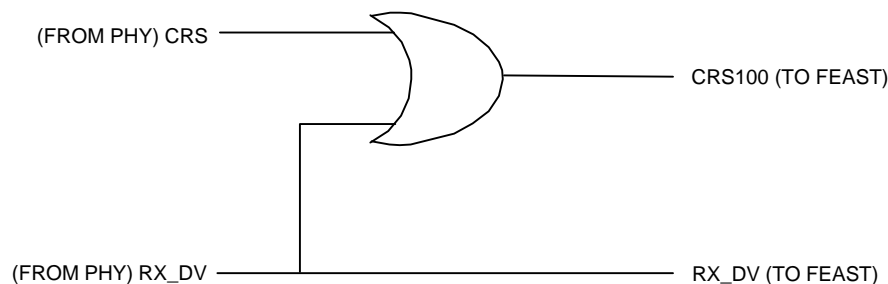
For the LAN91C110 INTR1, INTR2 and INTR3 Pins have been removed. In order for software that uses interrupts to work properly with the LAN91C110, both INT SEL 0-1 bits in Configuration register should be 0 regardless of the interrupt number (IRQ) used in the host.

Working around Carrier Sense issue in full duplex

This section discusses an issue observed when using either the LAN91C100FD and LAN91C110 chips and the possible workarounds.

When operating in full duplex the LAN91C1XX chips expect to see the Carrier Sense signal asserted (by the PHY) even when operating in full duplex mode. It has been observed that some PHYs assert this signal on receives, some do not, and some have a control to select the presence or lack of assertion.

- For those PHYs that always assert CRS on full duplex there is no workaround needed.
- For those PHYs that have a control for the behavior of CRS on receives, it needs to be set to the selection in which CRS is asserted. For example this behavior is achieved in the LAN83C180 PHY by setting bit 5 (0x20) in PHY register offset 0x18.
- For those PHYs that do not provide any mechanism to enable the assertion of CRS on full duplex receives, a hardware solution can be implemented. The CRS_100 pin in the LAN91C1XX should be connected to the output of an OR gate of which the inputs are the CRS and RX_DV outputs from the PHY.





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