



APPLICATION NOTE 9.9

SMSC USB97CFDC Power-On-Reset Timing

Embedded Products Department Document #20010620HC

PRELIMINARY

Rev. 06/20/2001



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1 INTRODUCTION

This application note provides guidelines for USB97CFDC Power-On-Reset Timing when the Host momentarily interrupts power to the device while being in the suspend state.

1.1 Description

USB specification 1.1 states that the host should not remove power from the device while in suspend state. If the power is interrupted to the USB97CFDC under a suspend state, it may cause the device to power up in an unknown state or may not even come out of suspend state. The brief interruption in power to the device never allows the supply on the device to go low enough (below 0.4V for 10ms) before the internal POR (power on reset) circuit can reset the device properly. In some customer's designs, the power supply regulator output capacitor does not allow a fast enough discharge to allow the internal POR signal to be generated, but does allow the nRESET to be activated, resetting other parts of the USB97CFDC. This internal POR signal is needed to clear an internal PLL power-down bit that is set before going into suspend state by the firmware and is needed for the PLL re-arm.

To guarantee that the USB97CFDC starts up in a known state or comes out of the suspend state properly; the internal PLL power-down bit must be cleared after power is applied to the USB97CFDC. This is accomplished by tying pin 16 (nTESTEN) to the system reset pin 21 (nRESET) as shown in figure 1. In systems where there is not the possibility of nRESET being generated without the VDD to the USB97CFDC remaining low for at least 10ms, pin 16 can be tied to VDD as shown in the USB97CFDC reference designs. But in those systems where nRESET can occur without VDD remaining low for 10ms, then pin 16 should be tied to nRESET.

Note: nRESET must remain low for at least 15ms after VDD to the device rises to specification levels.

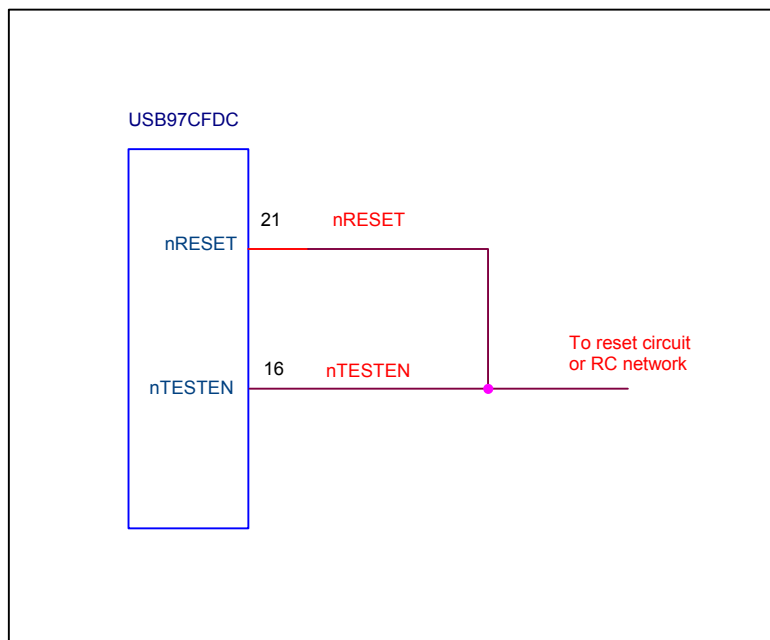


FIGURE 1 – POWER ON RESET CIRCUIT

2 SUMMARY

SMSC only recommends implementing the above hardware solution in order to avoid POR problems when an interrupt in power to the device during suspend state is abruptly caused by the host and a nRESET pulse is generated by the application circuit before the VDD to the device can reduce to a minimum and remain low for 10ms. For typical applications where the nRESET pulse is generated only after the VDD is low for 10ms or longer, pin 16 (nTESTEN) may be tied high.