

COM20051+ Watchdog Timer Register Definitions

The COM20051+ incorporates a Watchdog Timer which is explained in the COM20051+ data sheet. This application note clarifies the Watchdog Timer Register Definitions.

COM20051+ Watchdog Timer Registers have the following layout:

WATCHDOG REGISTER 1 (WD1REG): Offset = +0Ah, Default value = 00h

READ/WRITE

(This register has the same function when reading it or writing to it)

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0

WATCHDOG REGISTER 2 (WD2REG): Offset = + 0Bh, Default value = 00h

(The bits in this register have different functions depending whether the register is read or written to)

WRITE

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
x	TEST	51RESET	WDRESET	ENABLE	TD10	TD9	TD8

READ

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	TEST	51RESET	STROBE	ENABLE	TD10	TD9	TD8

BIT DEFINITIONS:

BIT NAME	BIT DESCRIPTION
TD10 - TD0	Time Divisor. Defaults to 0
ENABLE	Watchdog Timer Enable. After this bit is set to logic "1", the Watchdog Timer will start counting up to the value set by the Time Divisor.
WDRESET	Watchdog Reset. Bit 4 of WD2REG. Writing the WD2REG with this bit set to logic "1" will reset the Watchdog Timer's counter, and the Watchdog Timer will stop.
STROBE	Watchdog Strobe. Bit 4 of WD2REG. Reading the WD2REG will remove the Watchdog Timer's counter reset condition and Watchdog Timer will restart.
51RESET	COM20051+ Reset Mode. If this bit is a logic "0" - Watchdog Timer will provide only a 3.2 μ s reset pulse to the COM20051+. If this bit is a logic "1", the Watchdog Timer will hold the COM220051+ in reset until the hardware reset is applied.
TEST	Test Bit. If set to a logic "1", it will enable the output of the STROBE bit state on Port 1.0.



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