



# High-Performance Single-Chip 10/100 Ethernet Controller with HP Auto-MDIX Support

## PRODUCT FEATURES

Data Brief

### Highlights

- Optimized for the highest performance applications
- Efficient architecture with low CPU overhead
- Easily interfaces to most 32-bit and 16-bit embedded CPU's
- Integrated PHY with HP Auto-MDIX support
- Supports audio & video streaming over Ethernet: multiple high-definition (HD) MPEG2 streams
- Compatible with other members of LAN9218 family

### Target Applications

- Video distribution systems, multi-room PVR
- Cable, satellite, and IP set-top boxes
- Digital video recorders and DVD recorder/players
- Digital TV
- Digital media clients/servers and home gateways
- Video-over IP solutions, IP PBX & video phones
- Wireless routers & access points
- High-end audio distribution systems

### Key Benefits

- Non-PCI Ethernet controller for the highest performance applications
  - Highest performing non-PCI Ethernet controller
  - 32-bit interface with fast bus cycle times
  - Burst-mode read support
- Eliminates dropped packets
  - Internal buffer memory can store over 200 packets
  - Automatic PAUSE and back-pressure flow control
- Minimizes CPU overhead
  - Supports Slave-DMA
  - Interrupt Pin with Programmable Hold-off timer
- Reduces system cost and increases design flexibility
- SRAM-like interface easily interfaces to most embedded CPU's or SoC's

- Reduced Power Modes
  - Numerous power management modes
  - Wake on LAN\*
  - Magic packet wakeup\*
  - Wakeup indicator event signal
  - Link Status Change
- Single chip Ethernet controller
  - Fully compliant with IEEE 802.3/802.3u standards
  - Integrated Ethernet MAC and PHY
  - 10BASE-T and 100BASE-TX support
  - Full- and Half-duplex support
  - Full-duplex flow control
  - Backpressure for half-duplex flow control
  - Preamble generation and removal
  - Automatic 32-bit CRC generation and checking
  - Automatic payload padding and pad removal
  - Loop-back modes
- Flexible address filtering modes
  - One 48-bit perfect address
  - 64 hash-filtered multicast addresses
  - Pass all multicast
  - Promiscuous mode
  - Inverse filtering
  - Pass all incoming with status report
  - Disable reception of broadcast packets
- Integrated 10/100 Ethernet PHY
  - Supports HP Auto-MDIX
  - Auto-negotiation
  - Supports energy-detect power down
- Host bus interface
  - Simple, SRAM-like interface
  - 32 or 16-bit data bus
  - 16Kbyte FIFO with flexible TX/RX allocation
  - One configurable host interrupt
- Miscellaneous features
  - Low-profile 100-pin TQFP, lead-free RoHS Compliant package
  - Integrated 1.8V regulator
  - General Purpose Timer
  - Optional EEPROM interface
  - Support for 3 status LEDs multiplexed with Programmable GPIO signals
- Single 3.3V Power Supply with 5V tolerant I/O
- 0°C to +70°C Commercial Temperature Support

\* Third-party brands and names are the property of their respective owners.

**ORDER NUMBER(S):****LAN9218-MT FOR 100-PIN, TQFP LEAD-FREE ROHS COMPLIANT PACKAGE WITH E3 FINISH (MATTE TIN)  
(0 TO +70°C TEMP RANGE)**

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## General Description

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The LAN9218 is a full-featured, single-chip 10/100 Ethernet controller designed for embedded applications where performance, flexibility, ease of integration and system cost control are required. The LAN9218 has been specifically architected to provide the highest performance possible for any given architecture. The LAN9218 is fully IEEE 802.3 10BASE-T and 802.3u 100BASE-TX compliant, and supports HP Auto-MDIX.

The LAN9218 includes an integrated Ethernet MAC and PHY with a high-performance SRAM-like slave interface. The simple, yet highly functional host bus interface provides a glue-less connection to most common 16-bit and 32-bit microprocessors and microcontrollers. The LAN9218 includes large transmit and receive data FIFOs with a high-speed host bus interface to accommodate high bandwidth, high latency applications. In addition, the LAN9218 memory buffer architecture allows highly efficient use of memory resources by optimizing packet granularity.

### Applications

The LAN9218 is well suited for many high performance embedded applications, including:

- High-end cable, satellite and IP set-top boxes
- Video distribution systems
- Multi-room PVR (Personal Video Recorder)
- Digital video recorders
- High-definition televisions
- Digital media clients/servers
- Home gateways

The LAN9218 also supports features which reduce or eliminate packet loss. Its internal 16-KByte SRAM can hold over 200 received packets. If the receive FIFO gets too full, the LAN9218 can automatically generate flow control packets to the remote node, or assert back-pressure on the remote node by generating network collisions.

The LAN9218 supports numerous power management and wakeup features. The LAN9218 can be placed in a reduced power mode and can be programmed to issue an external wake signal via several methods, including "Magic Packet", "Wake on LAN" and "Link Status Change". This signal is ideal for triggering system power-up using remote Ethernet wakeup events. The device can be removed from the low power state via a host processor command.

## Block Diagram

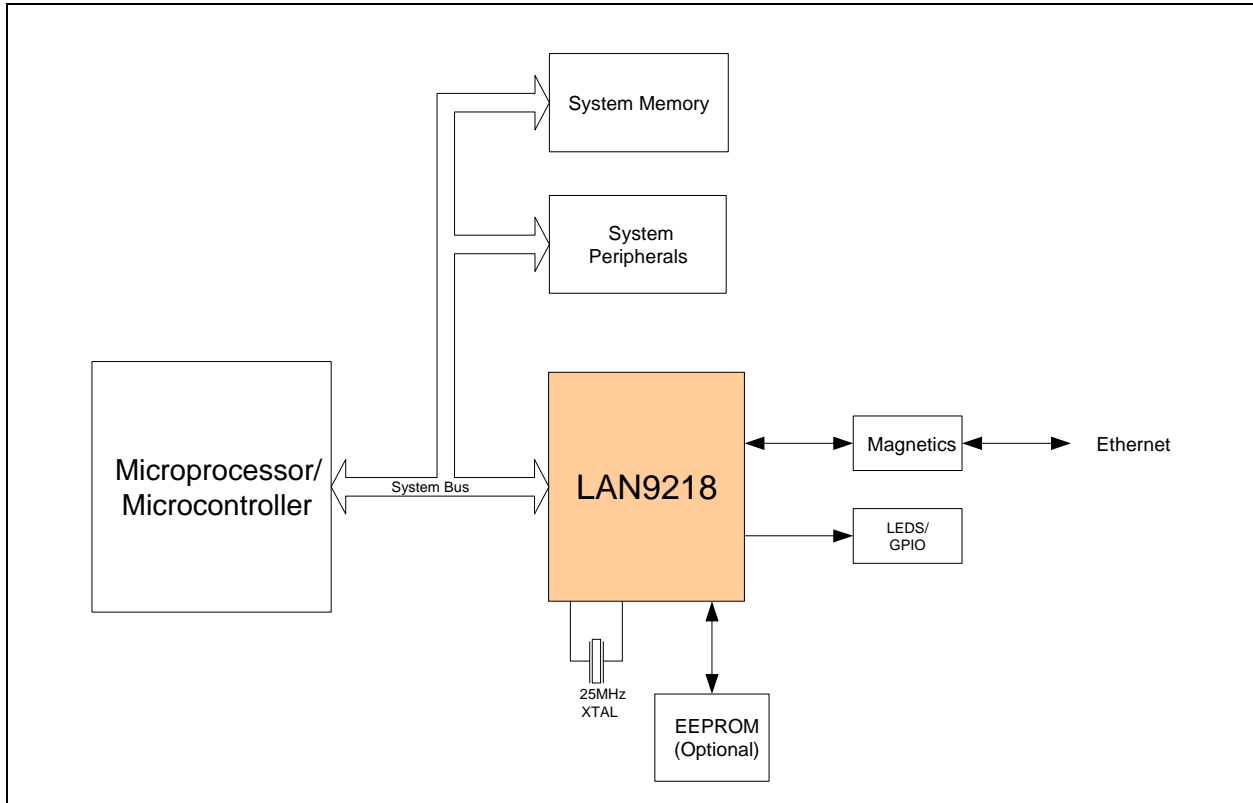


Figure 1 System Block Diagram

## Package Outline

### 100-TQFP Package

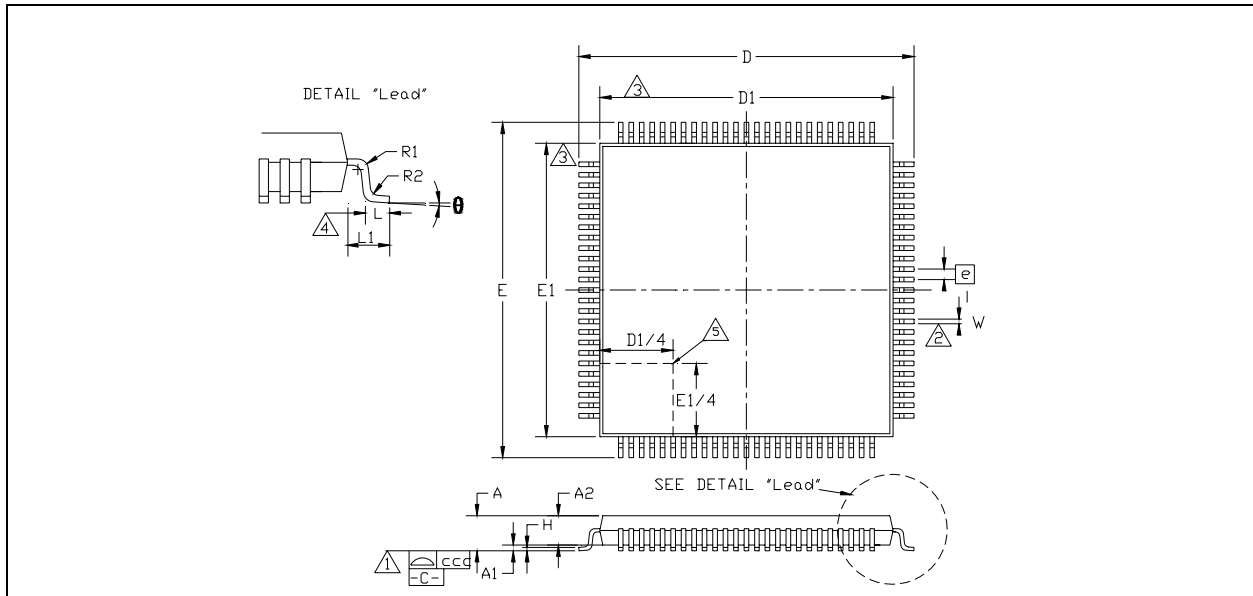


Figure 2 100 Pin TQFP Package Definition

Table 1 100 Pin TQFP Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	~	~	1.60	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	1.35	~	1.45	Body Thickness
D	15.80	~	16.20	X Span
D1	13.90	~	14.10	X body Size
E	15.80	~	16.20	Y Span
E1	13.90	~	14.10	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length
L1	~	1.00	~	Lead Length
e	0.50 Basic			Lead Pitch
q	0°	~	7°	Lead Foot Angle
W	0.17	0.22	0.27	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

**Notes:**

- Controlling Unit: millimeter.
- Tolerance on the true position of the leads is  $\pm 0.04$  mm maximum.
- Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25 mm.
- Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
- Details of pin 1 identifier are optional but must be located within the zone indicated.