



## LAN9500/LAN9500i

# Hi-Speed USB 2.0 to 10/100 Ethernet Controller

## PRODUCT FEATURES

Data Brief

### Highlights

- Single Chip Hi-Speed USB 2.0 to 10/100 Ethernet Controller
- Integrated 10/100 Ethernet MAC with Full-Duplex Support
- Integrated 10/100 Ethernet PHY with HP Auto-MDIX support
- Integrated USB 2.0 Hi-Speed Device Controller
- Integrated USB 2.0 Hi-Speed PHY
- Implements Reduced Power Operating Modes

### Target Applications

- Embedded Systems
- Set-Top Boxes
- PVR's
- CE Devices
- Networked Printers
- USB Port Replicators
- Standalone USB to Ethernet Dongles
- Test Instrumentation
- Industrial

### Key Benefits

- USB Device Controller
  - Fully compliant with Hi-Speed Universal Serial Bus Specification Revision 2.0
  - Supports HS (480 Mbps) and FS (12 Mbps) modes
  - Four endpoints supported
  - Supports vendor specific commands
  - Integrated USB 2.0 PHY
  - Remote wakeup supported
- High-Performance 10/100 Ethernet Controller
  - Fully compliant with IEEE802.3/802.3u
  - Integrated Ethernet MAC and PHY
  - 10BASE-T and 100BASE-TX support
  - Full- and half-duplex support
  - Full- and half-duplex flow control

- Preamble generation and removal
- Automatic 32-bit CRC generation and checking
- Automatic payload padding and pad removal
- Loop-back modes
- TCP/UDP/IP/ICMP checksum offload support
- Flexible address filtering modes
  - One 48-bit perfect address
  - 64 hash-filtered multicast addresses
  - Pass all multicast
  - Promiscuous mode
  - Inverse filtering
  - Pass all incoming with status report
- Wakeup packet support
- Integrated Ethernet PHY
  - Auto-negotiation
  - Automatic polarity detection and correction
  - HP Auto-MDIX support
  - Link status change wake-up detection
- Support for 3 status LEDs
- External MII to support HomePNA™ and HomePlug® PHY
- Power and I/Os
  - Various low power modes
  - 11 GPIOs
  - Supports bus-powered and self-powered operation
  - Integrated power-on reset circuit
  - External 3.3v I/O supply
    - Internal 1.8v core supply regulator
- Miscellaneous Features
  - EEPROM Controller
  - IEEE 1149.1 (JTAG) Boundary Scan
  - Requires single 25 MHz crystal
- Software
  - Windows XP/Vista Driver
  - Linux Driver
  - Win CE Driver
  - MAC OS Driver
  - EEPROM Utility
- Packaging
  - 56-pin QFN (8x8 mm) Lead-Free RoHS Compliant package
- Environmental
  - Commercial Temperature Range (0°C to +70°C)
  - Industrial Temperature Range (-40°C to +85°C)

**ORDER NUMBER(S):**

**LAN9500-ABZJ FOR 56-PIN, QFN LEAD-FREE ROHS COMPLIANT PACKAGE (0 TO +70°C TEMP RANGE)**  
**LAN9500i-ABZJ FOR 56-PIN, QFN LEAD-FREE ROHS COMPLIANT PACKAGE (-40 TO +85°C TEMP RANGE)**



80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000, FAX (631) 273-3123

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## General Description

The LAN9500/LAN9500i is a high performance Hi-Speed USB 2.0 to 10/100 Ethernet controller. With applications ranging from embedded systems, set-top boxes, and PVR's, to USB port replicators, USB to Ethernet dongles, and test instrumentation, the LAN9500/LAN9500i is a high performance and cost competitive USB to Ethernet connectivity solution.

The LAN9500/LAN9500i contains an integrated 10/100 Ethernet PHY, USB PHY, Hi-Speed USB 2.0 device controller, 10/100 Ethernet MAC, TAP controller, EEPROM controller, and a FIFO controller with a total of 30 KB of internal packet buffering.

The internal USB 2.0 device controller and USB PHY are compliant with the USB 2.0 Hi-Speed standard. The LAN9500/LAN9500i implements Control, Interrupt, Bulk-in, and Bulk-out USB Endpoints.

The Ethernet controller supports auto-negotiation, auto-polarity correction, HP Auto-MDIX, and is compliant with the IEEE 802.3 and IEEE 802.3u standards. An external MII interface provides support for an external Fast Ethernet PHY, HomePNA, and HomePlug functionality.

Multiple power management features are provided, including various low power modes and "Magic Packet", "Wake On LAN", and "Link Status Change" wake events. These wake events can be programmed to initiate a USB remote wakeup.

An internal EEPROM controller exists to load various USB configuration information and the device MAC address. The integrated IEEE 1149.1 compliant TAP controller provides boundary scan via JTAG.

## Block Diagram

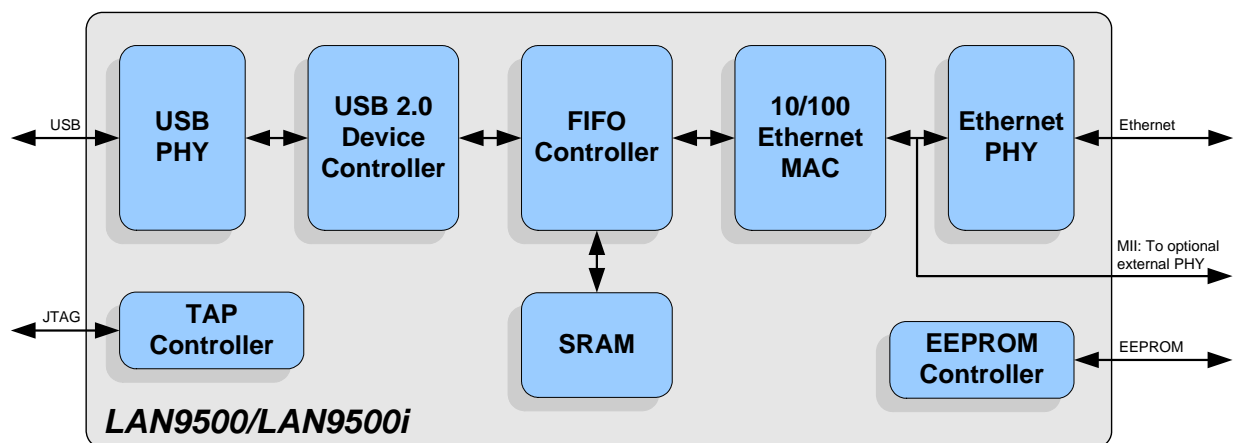
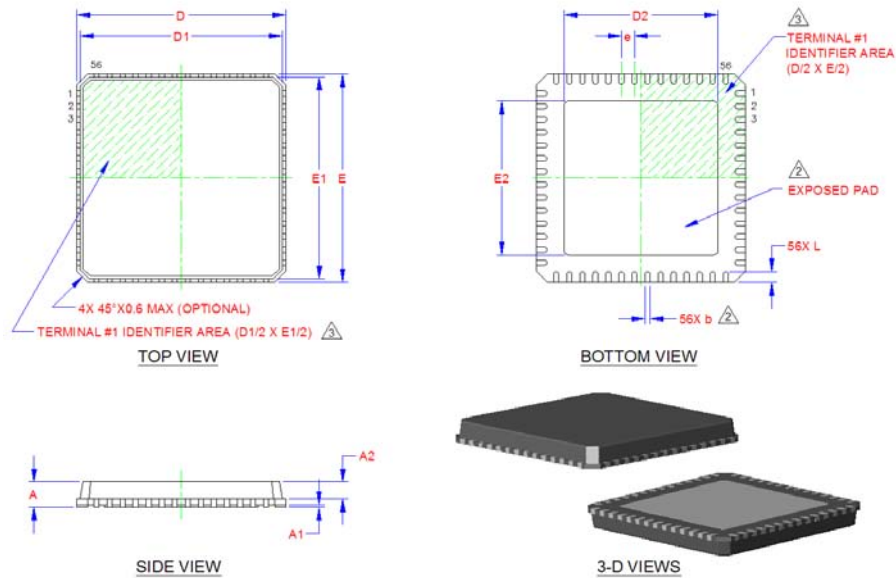


Figure 1 LAN9500/LAN9500i Block Diagram

# Package Outline



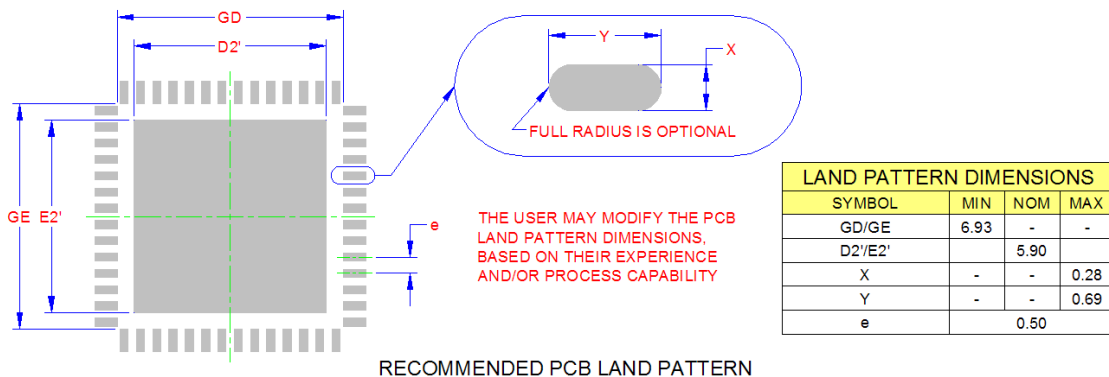
**Figure 2 LAN9500/LAN9500i 56-QFN Package**

**Table 1 LAN9500/LAN9500i 56-QFN Dimensions**

	MIN	NOMINAL	MAX	REMARKS
A	0.70	-	1.00	Overall Package Height
A1	0.00	0.02	0.05	Standoff
A2	-	-	0.90	Mold Cap Thickness
D/E	7.85	8.00	8.15	X/Y Body Size
D1/E1	7.55	-	7.95	X/Y Mold Cap Size
D2/E2	5.75	5.90	6.05	X/Y Exposed Pad Size
L	0.30	-	0.50	Terminal Length
b	0.18	0.25	0.30	Terminal Width
e	0.50 BSC			Terminal Pitch

**Notes:**

1. All dimensions are in millimeters unless otherwise noted.
2. Position tolerance of each terminal and exposed pad is +/- 0.05 mm at maximum material condition. Dimension "b" applies to plated terminals and is measured between 0.15 and 0.30 mm from the terminal tip.
3. The pin 1 identifier may vary, but is always located within the zone indicated.



**Figure 3 LAN9500/LAN9500i 56-QFN Recommended PCB Land Pattern**