

EVB-LAN8187

LAN8187 MII(i) Customer Evaluation Board

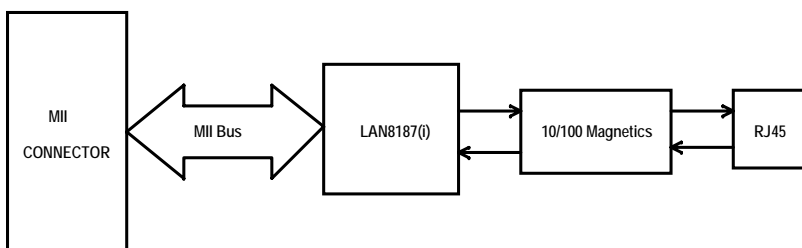
Design Details

Schematic Revision A1

Board: PCB-7058AZ-A
Chip: LAN8187(i)
Board Form Factor:
Assembly:

Circuit Diagrams utilizing SMSC Products Are Included As A Means Of Illustrating Typical Semiconductor Applications: Consequently Complete Information Sufficient For Construction Purposes Is Not Necessarily Given. The Information Has Been Carefully Checked And Is Believed To Be Entirely Reliable. However, No Responsibility Is Assumed For Inaccuracies. Furthermore, Such Information Does Not Convey To The Purchaser Of The Semiconductor Devices Described Any License Under The Patent Rights Of SMSC Or Others. SMSC Reserves The Right To Make Changes At Any Time In Order To Improve Design And Supply The Best Product Possible.

EVB BLOCK DIAGRAM



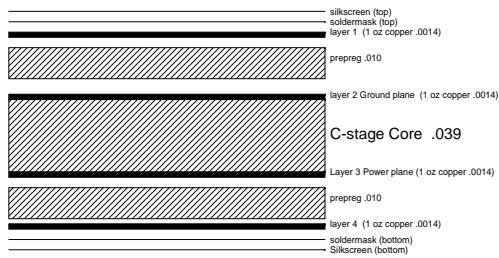
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Revisions
Rev A1 Modified for Public release



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stackup



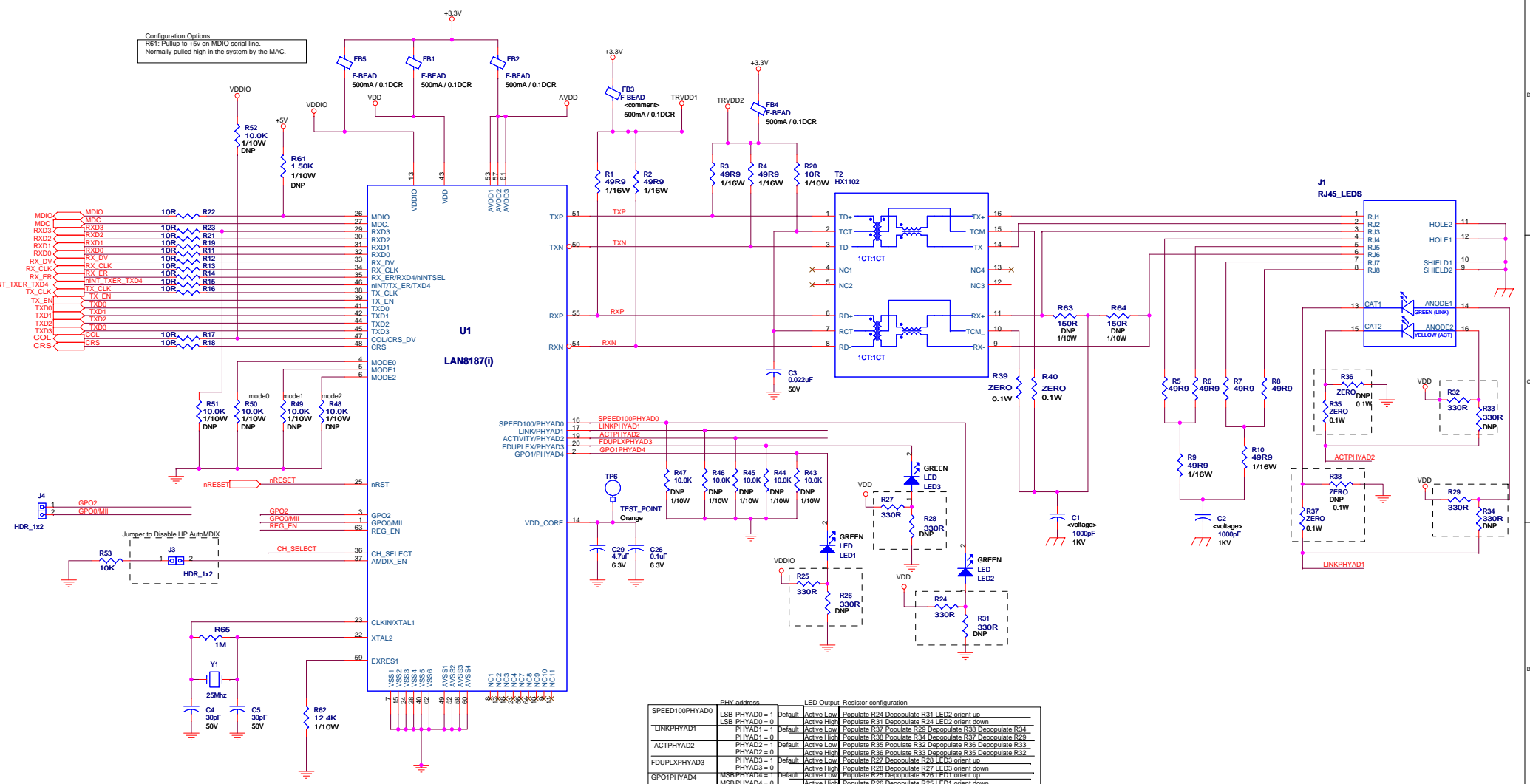
NOTES:

- BOARD FABRICATION AND QUALITY ACCEPTANCE PER IPC-6012 CLASS 2. BOARD MUST MEET OR EXCEED QUALIFICATION TESTING AND QUALITY CONFORMANCE TESTING INSPECTION SPECIFIED WITHIN.
- MATERIAL: NEMA GRADE STANDARD FR4 LAMINATED SHEET; HTE 1 OZ COPPER CLAD, TYPE GF/GF3 WOVEN GLASS BASE; FLAME RESISTANCE MEETING UL94V-0 OR BETTER. MATERIAL IN ACCORDANCE WITH IPC-4101.
- BOARD FABRICATION SHALL APPLY DATE CODE, FABRICATOR'S CAGE CODE, I.D. AND UL MARKING TO SECONDARY SIDE WHERE INDICATED. MARKING PREFERABLY COPPER ETCHED, EPOXY INK ACCEPTABLE.
- SOLDERMASK USING TYPE B PHOTO IMAGEABLE LPI FILM 0.0015 THICK. APPLY TO BOTH SIDES IN ACCORDANCE WITH IPC-SM-840 (TYPE B CLASS 3). USE APPROPRIATE SOLDER MASK ARTWORK FOR EACH SIDE. PUNCTURING OF PUNCTURING OF TENDED HOLES IS PERMISSIBLE. SOLDERMASK MISREGISTRATION SHALL NOT EXCEED .004 INCH. SOLDERMASK OVERLAP PERMITTED ON CIRCULAR LANDS ONLY AND SHALL NOT EXCEED 0.001 INCH. NO OVERLAP PERMITTED ON RECTANGULAR LANDS.
- FINISH: SOLDER MASK OVER BARE COPPER (SMOBC), HOT AIR LEVEL DEPOSIT ABOUT TRUE POSITION.
- DRILL BOARDS USING DRILL DATA, DRILL PATTERN AND HOLE SCHEDULE. HOLE LOCATION MAY VARY WITHIN .004 IN. MAX.
- MINIMUM ANNULAR RINGS: .002 IN MINIMUM - EXTERNAL LAYERS. .001 IN MINIMUM - INTERNAL LAYERS.
- ALL EXPOSED SURFACE LANDS AND LINES TO BE SOLDER COATED.
- ALL HOLES ARE PLATED THROUGH UNLESS NOTED OTHERWISE. MINIMUM COPPER PLATING IN PLATED HOLES TO BE .001 IN. COPPER PLATING IN TENDED HOLES SHALL NOT PLUG HOLES WITHOUT PERMISSION FROM SMSC.
- COMPONENT MARKINGS: SILKSCREEN BOTH SIDES USING NON-CONDUCTIVE WHITE EPOXY INK. LANDS AND EXPOSED PLATED AREAS TO BE FREE OF INK.
- DIMENSIONS ARE AFTER ETCHING AND PLATING AND ARE BASIC UNLESS OTHERWISE INDICATED.
- BARE BOARD ELECTRICAL TEST: BARE BOARDS SHALL BE ELECTRICALLY TESTED USING CAD GENERATED NET LIST DATA. THIS INFORMATION TO BE SUPPLIED IN IPC-D-350 FORMAT. ELECTRICAL TESTING SHALL FOLLOW THE GUIDELINES ESTABLISHED BY IPC-ET-652. GUIDELINES AND REQUIREMENTS FOR ELECTRICAL TESTING OF PRINTED WIRING BOARDS.



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Configuration Options
 R51: Pullup to +5v on MDIO serial line.
 Normally pulled high in the system by the MAC.



Boot Strap Options

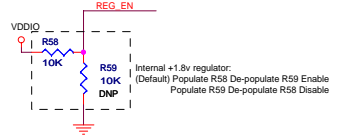
Mode 2	Mode 1	Mode 0	
R48	R49	R50	
Empty	Empty	Empty	111 All Capable (Default)
Empty	Empty	Populated	110 Power Down Mode
Empty	Populated	Empty	101 Repeater Mode
Empty	Populated	Populated	100 100Base-TX Half duplex Advertised
Populated	Empty	Empty	011 100Base-TX Full Duplex Auto Negotiate
Populated	Empty	Populated	010 100Base-TX Half Duplex Auto Negotiate
Populated	Populated	Empty	001 10Base-T Full Duplex Auto Negotiate
Populated	Populated	Populated	000 10Base-T Half Duplex Auto Negotiate

R51 Pin 48 mode

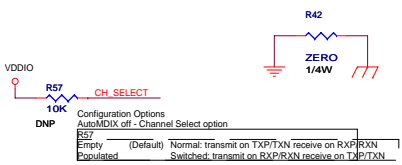
Empty	(Default) nINT
Populated	TXER/TXD4

Configuration Options
 Digital communications mode

R56	Populated
R57	(Default) MII mode
R58	Populated
R59	Populated



PHY address	LED Output	Resistor configuration
SPEED100PHYAD0	LSB PHYAD0 = 1	Default: Active Low; Populate R24 Depopulate R31 LED2 orient up
	LSB PHYAD0 = 0	Active High; Populate R31 Depopulate R24 LED2 orient down
LINKPHYAD1	PHYAD1 = 1	Default: Active Low; Populate R37 Populate R29 Depopulate R38 Depopulate R34
	PHYAD1 = 0	Active High; Populate R38 Populate R34 Depopulate R37 Depopulate R29
ACTPHYAD2	PHYAD2 = 1	Default: Active Low; Populate R35 Populate R32 Depopulate R36 Depopulate R33
	PHYAD2 = 0	Active High; Populate R36 Populate R33 Depopulate R35 Depopulate R32
FDUPLXPHYAD3	PHYAD3 = 1	Default: Active Low; Populate R27 Depopulate R28 LED3 orient up
	PHYAD3 = 0	Active High; Populate R28 Depopulate R27 LED3 orient down
GPO1PHYAD4	MSBPHYAD4 = 1	Default: Active Low; Populate R25 Depopulate R26 LED1 orient up
	MSBPHYAD4 = 0	Active High; Populate R26 Depopulate R25 LED1 orient down



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