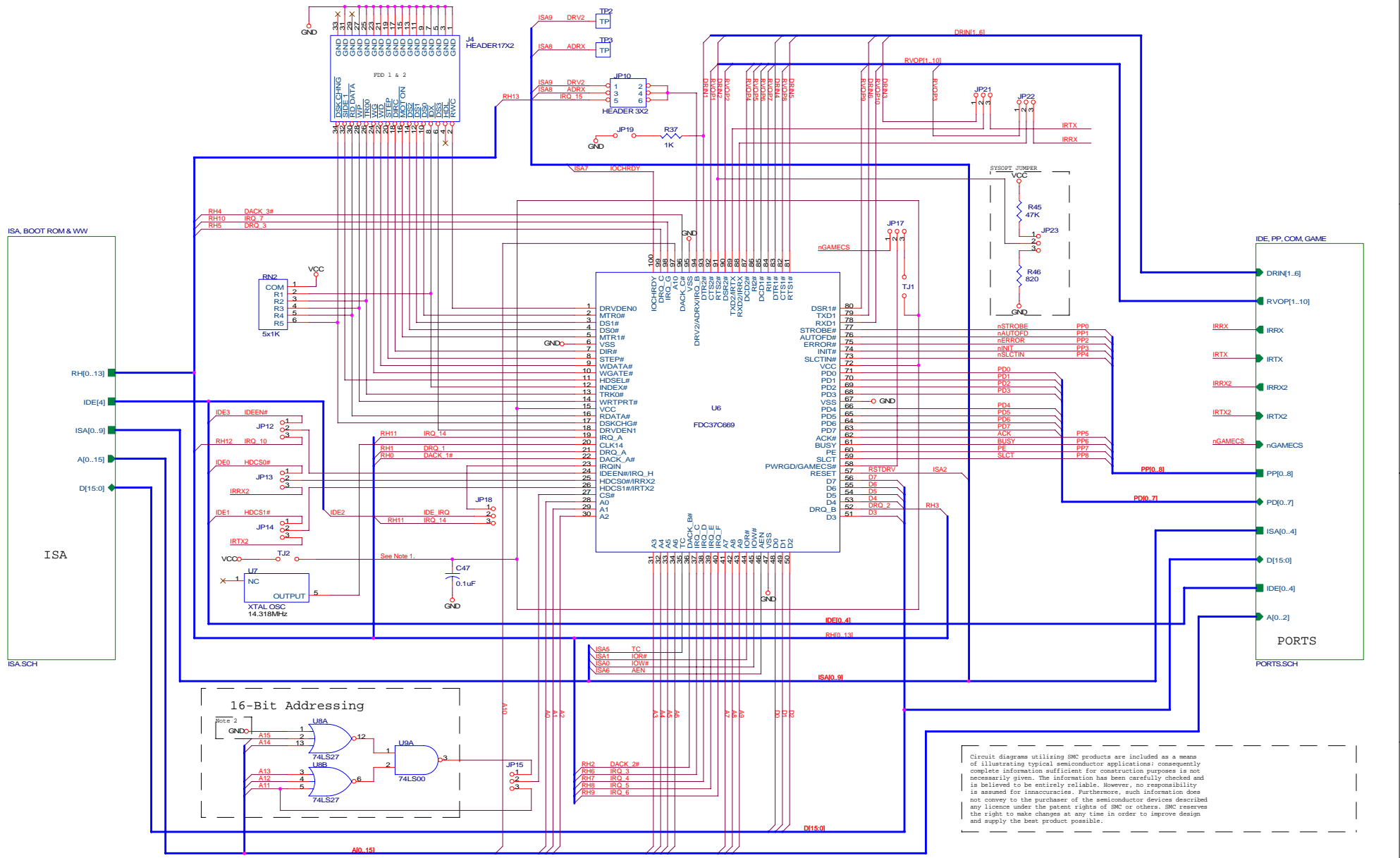


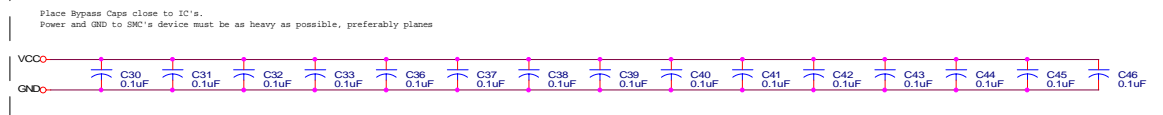
FDC37C669 SUPER I/O EVALUATION BOARD



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Note 1. Isolate the FDC37C669 VCC from the board VCC on the POWER layer. Connect this isolated supply to the board supply through the T1 jumper.

Note 2. This GND connection must be made on the Rev A EVB. The board presently has a connection to Vcc at this pin.



Designed using OrCAD 386+ v1.2

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