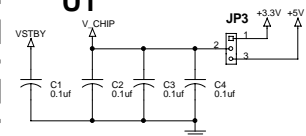
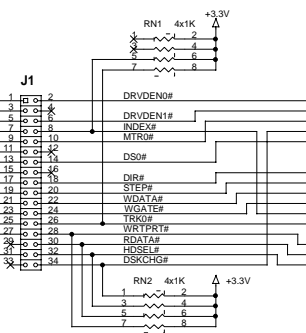


SMSC LPC47B27X REFERENCE DESIGN ASSY 6097 REV A1

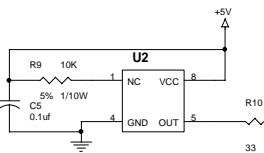
BYPASS FOR LPC47B27X, U1



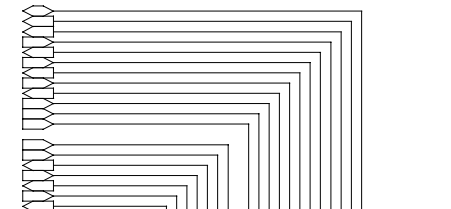
FLOPPY DRIVE 1



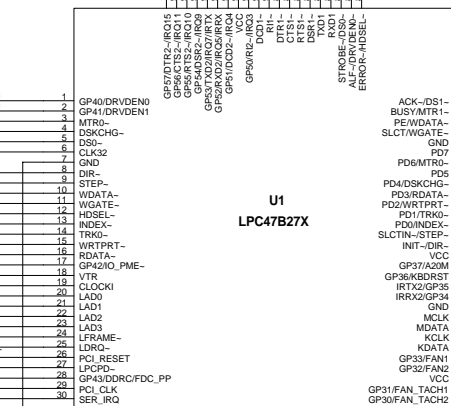
14.318Mhz CLOCK



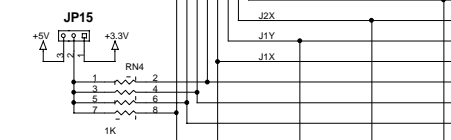
ERROR#
ALF#
STROBE#
RXD1
DSR1#
RTS1#
CTS1#
RT1#
DCD1#
R1#
DCD2#
R2#
DCD2#
RXD2
TXD2
DSR2#
R2R2#
CTS2#
DTR2#



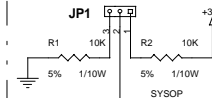
U1
LPC47B27X



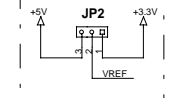
GAME PORT



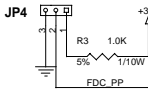
SYSOP



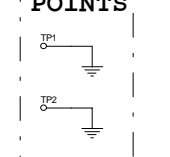
VREF



FPC / PP



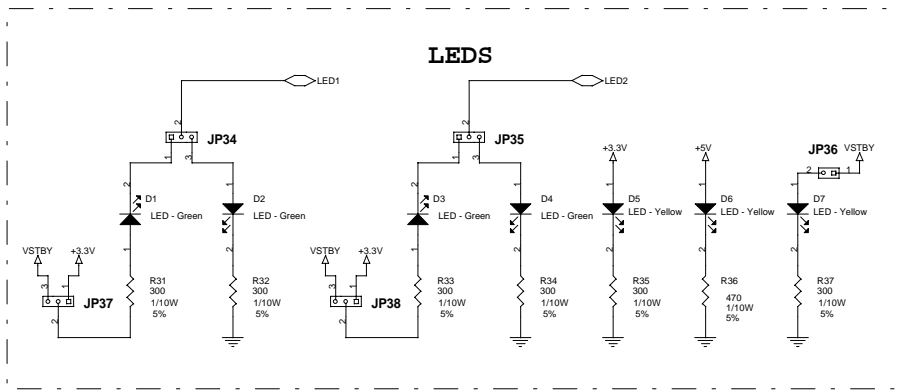
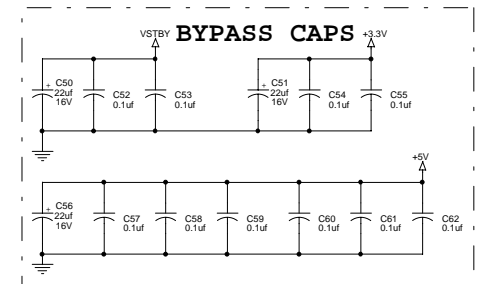
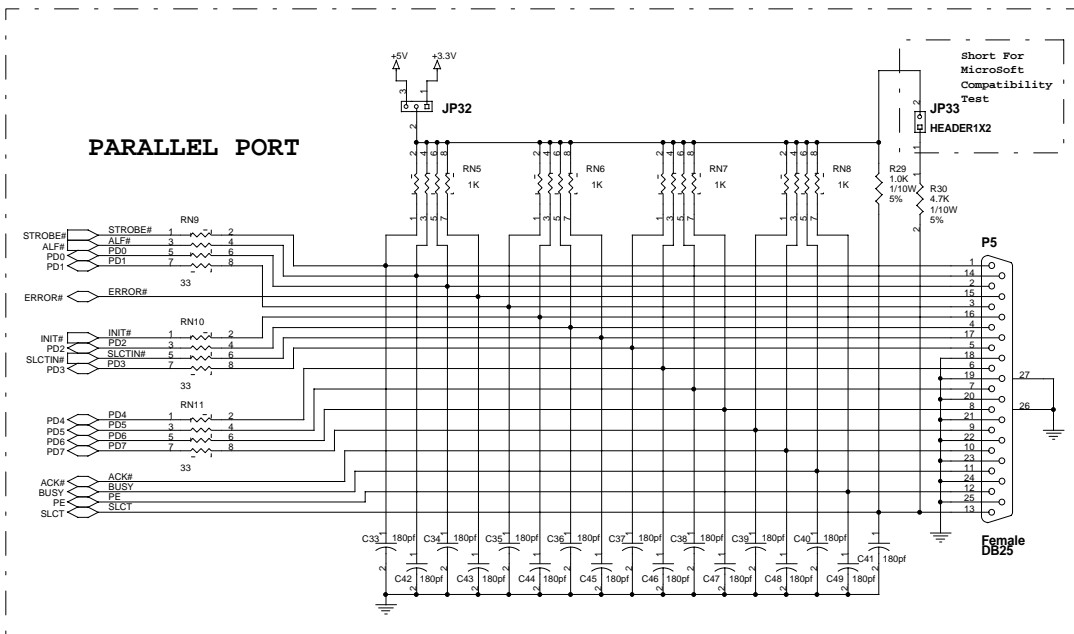
TEST POINTS



Provide
100 Pin
Breakout

Signal	Pin
DRV DEN0#	1
DRV DEN1#	2
INDEX#	3
DSKCHG#	4
DS0#	5
CLK32	6
GND	7
DIR#	8
STEP#	9
WDATA#	10
WGATE#	11
IRSEL#	12
INDEX#	13
TRK0#	14
WRTPRT#	15
RDATA#	16
PME#	17
VTR	18
CLOCK1	19
LAD0	20
LAD1	21
LAD2	22
LAD3	23
LFRAME#	24
LDR0#	25
PCI RESET	26
PCI CLK	27
PCI SER_IRQ	28
ACK#	29
BUSY	30
PE	31
SLCT	32
PD7	33
PD6	34
PD5	35
PD4	36
PD3	37
PD2	38
PD1	39
PD0	40
SLCTIN#	41
INIT#	42
INIT#	43
CHIP_A20	44
CHIP_KBDRST	45
IRTX2	46
IRRX2	47
MCLK	48
MDATA	49
KCLK	50
KDATA	51
FAN_TACH1	52
FAN_TACH2	53
IRTX2	54
IRRX2	55
MCLK	56
MDATA	57
KCLK	58
KDATA	59
GND	60
IRRX2	61
IRTX2	62
CHIP_KBDRST	63
CHIP_A20	64
V_CHIP	65
INIT#	66
SLCTIN#	67
PD0	68
PD1	69
PD2	70
PD3	71
PD4	72
PD5	73
PD6	74
PD7	75
GND	76
SLCT	77
PE	78
BUSY	79
ACK#	80
ERROR#	81
ALF#	82
STROBE#	83
RXD1	84
DSR1#	85
RTS1#	86
CTS1#	87
DTR1#	88
R1#	89
DCD1#	90
R2#	91
DCD2#	92
RXD2	93
TXD2	94
DSR2#	95
R2R2#	96
CTS2#	97
DTR2#	98
GND	99
DTR2#	100

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Date: Thursday, October 29, 1998	Sheet: 3	of 3