


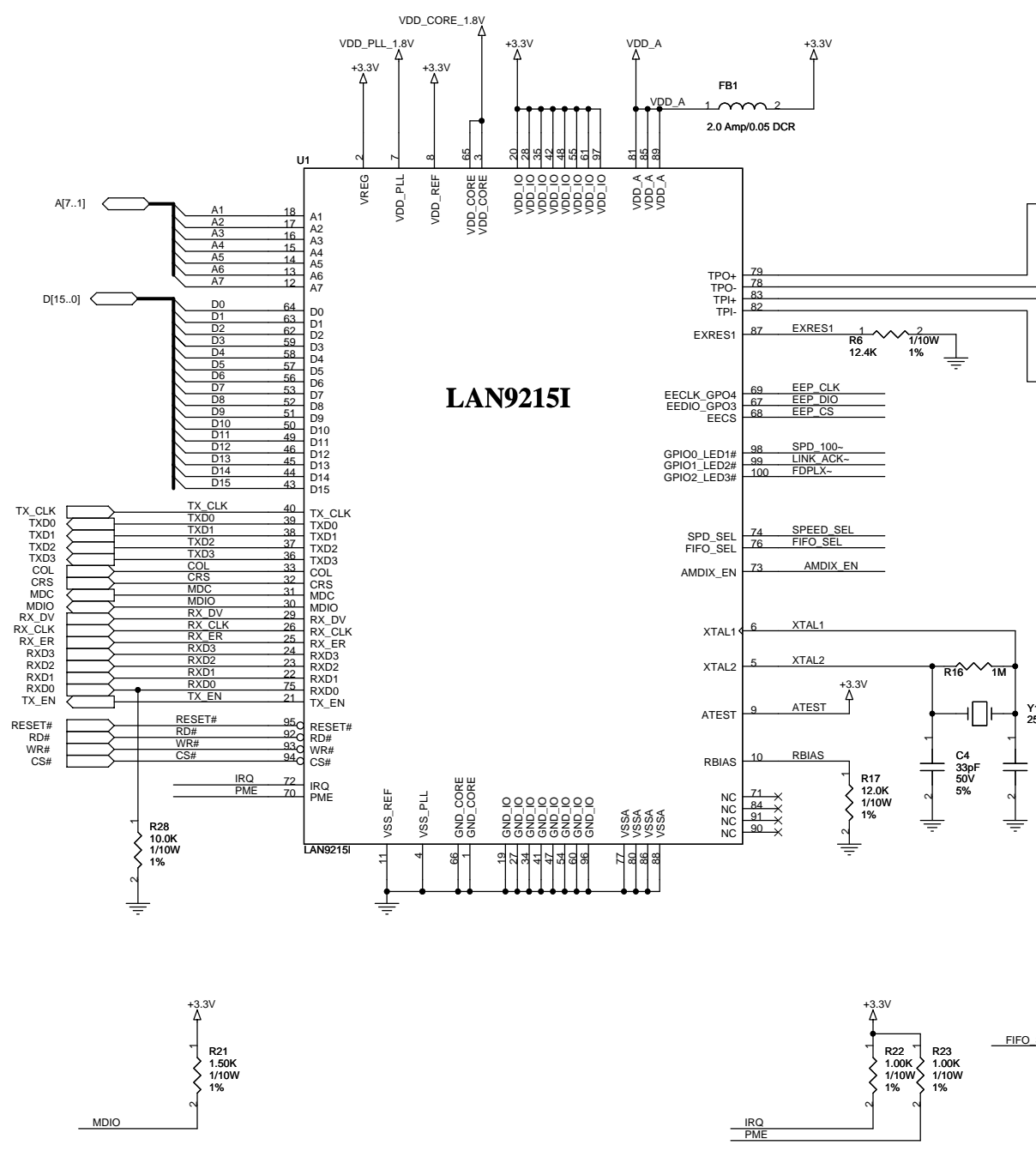
# LAN9215I Reference Schematic

Schematic Revision 0.5

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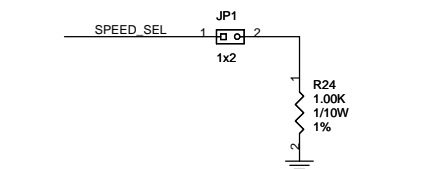
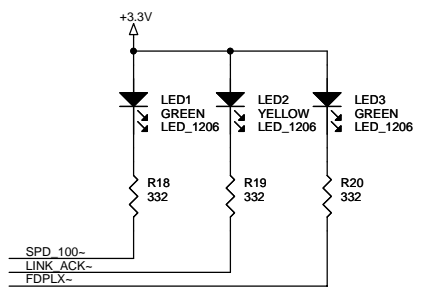
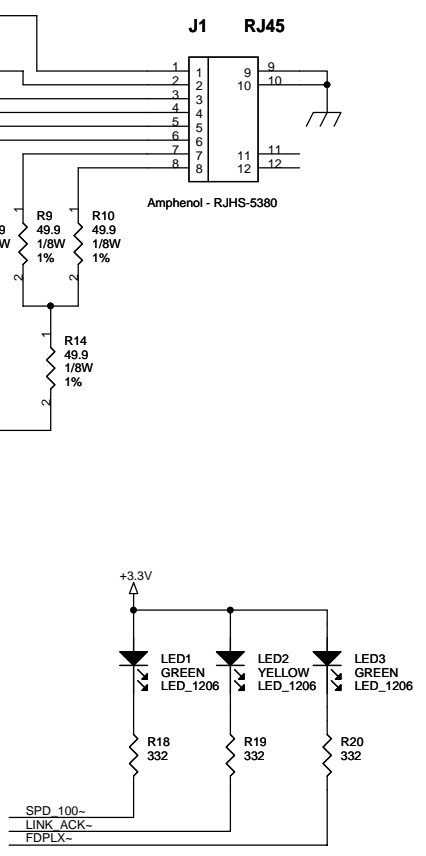
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Size C	Engineer N/A	Assembly No. N/A	Rev 0.5
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NOTE:  
25MHz Crystal Part Number is TBD.

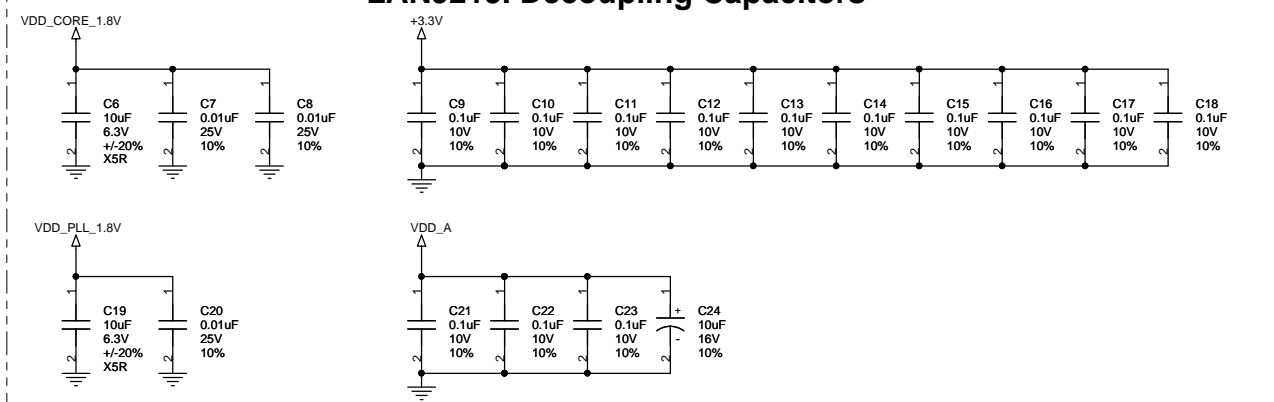
NOTE:  
FIFO\_SEL can be driven dynamically and is not pulled internally to either state. This pin has the same timing as the Address Bus and can be driven by upper address bits not used by the LAN9215I. Refer to datasheet.



NOTE:  
IN = 10Mbps, Half-Duplex, Auto Neg. Disabled  
OUT = 100Mbps, Half-Duplex, Auto Neg. Enabled

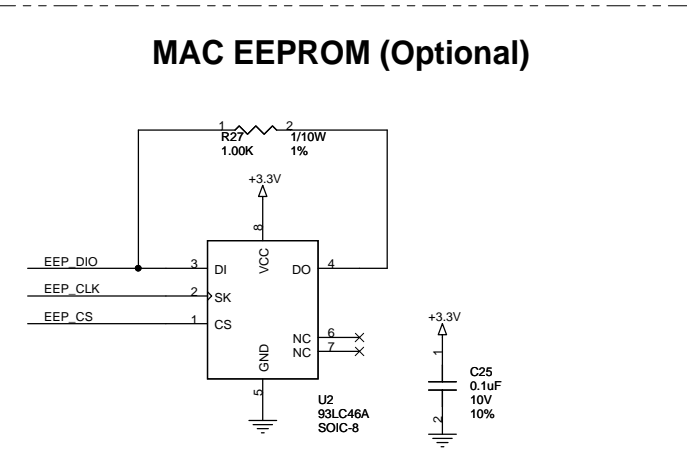
NOTE:  
IN = Auto-MDIX Functionality Enabled  
OUT = Auto-MDIX Functionality Disabled

### LAN9215I Decoupling Capacitors



NOTE:  
C6 and C19 must be low ESR capacitors. Ceramic is recommended.

### MAC EEPROM (Optional)



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Title: **LAN9215I Reference Schematic**

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