


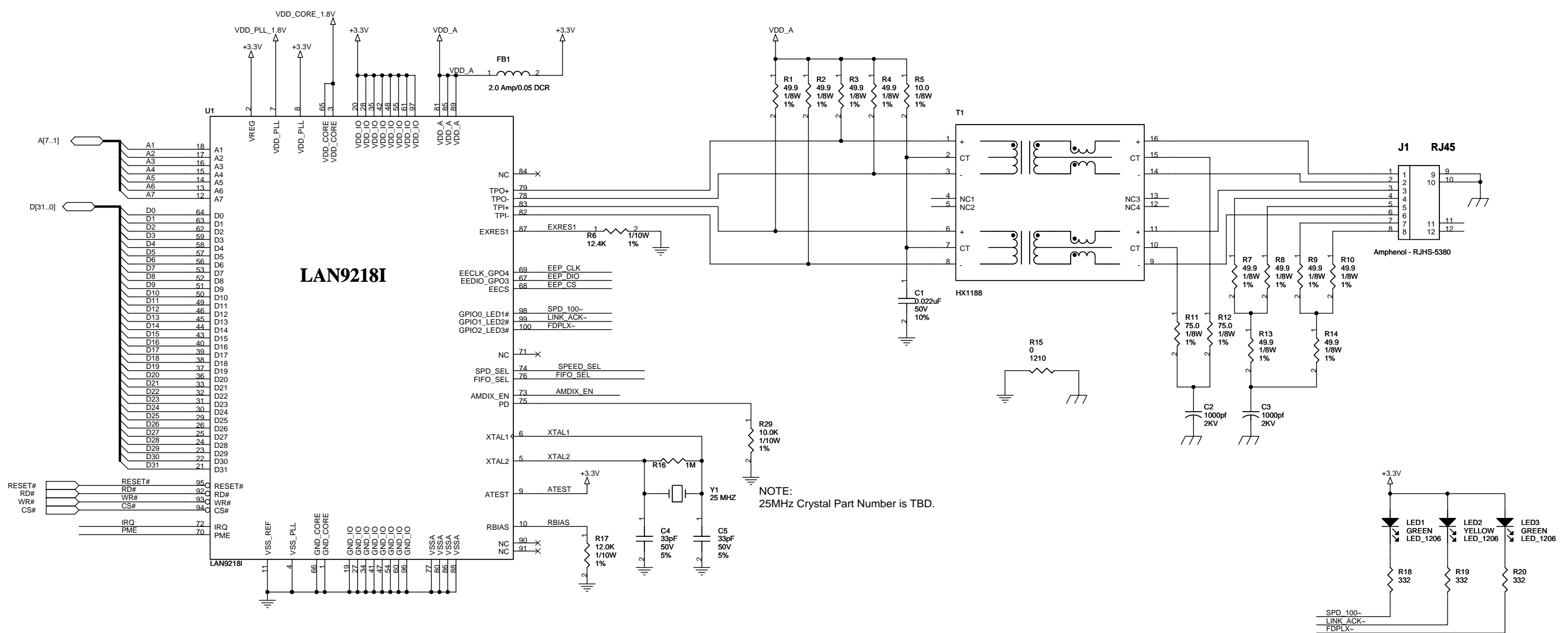
# LAN9218I Reference Schematic

Schematic Revision 0.5

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Circuit diagrams utilizing SMSC products are included as a means of illustrating typical semiconductor applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMSC or others. SMSC reserves the right to make changes at any time in order to improve design and supply the best product possible.

			
Title <b>LAN9218I Reference Schematic</b>			
Size C	Engineer N/A	Assembly No. N/A	Rev 0.5
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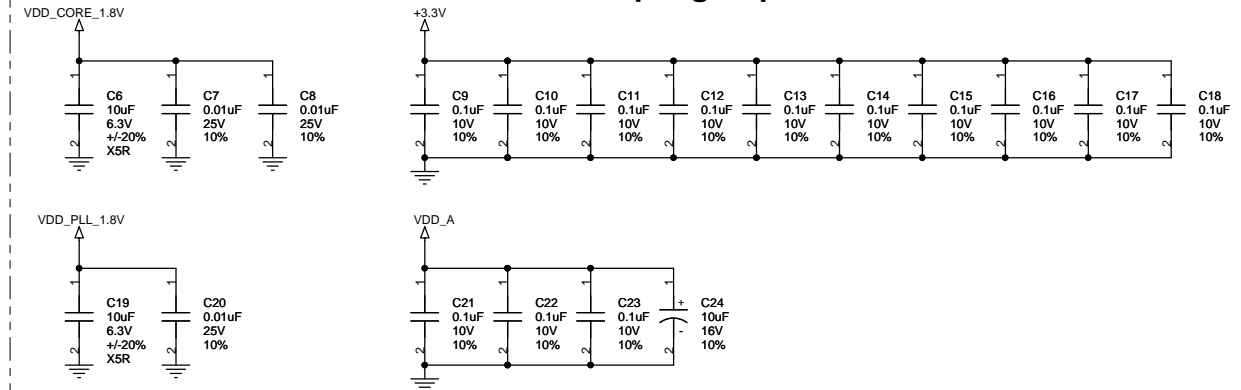
NOTE:  
25MHz Crystal Part Number is TBD.

NOTE:  
FIFO\_SEL can be driven dynamically and is not pulled internally to either state. This pin has the same timing as the Address Bus and can be driven by upper address bits not used by the LAN9218I. Refer to datasheet.

NOTE:  
IN = Auto-MDIX Functionality Enabled  
OUT = Auto-MDIX Functionality Disabled

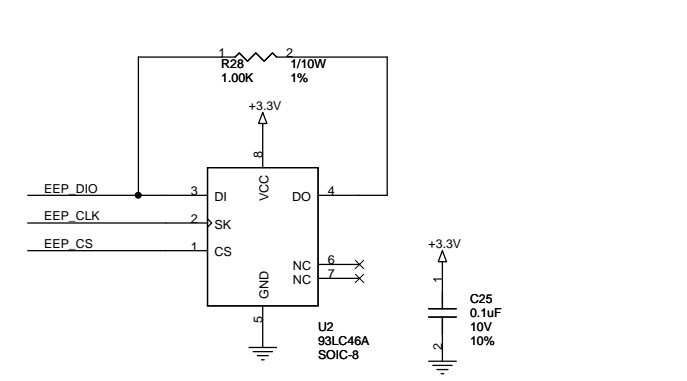
NOTE:  
EE\_DIO is the D32/D16# Strap  
1 - 2 = 32 Bit Mode  
2 - 3 = 16 Bit Mode

### LAN9218I Decoupling Capacitors



NOTE:  
C6 and C19 must be low ESR capacitors. Ceramic is recommended.

### MAC EEPROM (Optional)



NOTE:  
IN = 10Mbps, Half-Duplex, Auto Neg. Disabled  
OUT = 100Mbps, Half-Duplex, Auto Neg. Enabled

**SMSC**  
SUCCESS BY DESIGN

Title: **LAN9218I Reference Schematic**

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C	N/A	N/A	0.5

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