



SMSC[®]
SUCCESS BY DESIGN

LAN8187/LAN8187i



±15kV ESD Protected MII/RMII 10/100 Ethernet Transceiver with HP Auto-MDIX & flexPWR[®] Technology

PRODUCT FEATURES

Data Brief

- Single-Chip Ethernet Physical Layer Transceiver (PHY)
- ESD Protection levels of ±8kV HBM without external protection devices
- ESD protection levels of EN61000-4-2, ±8kV contact mode, and ±15kV for air discharge mode per independent test facility
- Comprehensive flexPWR[®] Technology
 - Flexible Power Management Architecture
- LVCMOS Variable I/O voltage range: +1.6V to +3.6V
- Integrated 3.3V to 1.8V regulator for optional single supply operation.
 - Regulator can be disabled if 1.8V system supply is available.
- Performs HP Auto-MDIX in accordance with IEEE 802.3ab specification
- Automatic Polarity Correction
- Latch-Up Performance Exceeds 150mA per EIA/JESD 78, Class II
- Energy Detect power-down mode
- Low Current consumption power down mode
- Low operating current consumption:
 - 39mA typical in 10BASE-T and
 - 79mA typical in 100BASE-TX mode
- Supports Auto-negotiation and Parallel Detection
- Supports the Media Independent Interface (MII) and Reduced Media Independent Interface (RMII)
- Compliant with IEEE 802.3-2005 standards
 - MII Pins tolerant to 3.6V
- IEEE 802.3-2005 compliant register functions
- Integrated DSP with Adaptive Equalizer
- Baseline Wander (BLW) Correction
- Vendor Specific register functions
- Low profile 64-pin TQFP lead-free RoHS compliant package (10 x 10 x 1.4mm)
- 4 LED status indicators
- Commercial Operating Temperature 0° C to 70° C
- Industrial Operating Temperature -40° C to 85° C version available (LAN8187i)

Applications

- Set Top Boxes
- Network Printers and Servers
- LAN on Motherboard
- 10/100 PCMCIA/CardBus Applications
- Embedded Telecom Applications
- Video Record/Playback Systems
- Cable Modems/Routers
- DSL Modems/Routers
- Digital Video Recorders
- Personal Video Recorders
- IP and Video Phones
- Wireless Access Points
- Digital Televisions
- Digital Media Adaptors/Servers
- POS Terminals
- Automotive Networking
- Gaming Consoles
- Security Systems
- Access Control

Order Numbers:

LAN8187-JT for 64-pin, TQFP Lead-Free RoHS Compliant Package

LAN8187i-JT for (Industrial Temp) 64-pin, TQFP Lead-Free RoHS Compliant Package



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General Description

The SMSC LAN8187/LAN8187i is a low-power, industrial temperature (LAN8187i), variable I/O voltage, analog interface IC with HP Auto-MDIX for high-performance embedded Ethernet applications. The LAN8187/LAN8187i can be configured to operate on a single 3.3V supply utilizing an integrated 3.3V to 1.8V linear regulator. An option is available to disable the linear regulator to optimize system designs that have a 1.8V power plane available.

Architectural Overview

The LAN8187/LAN8187i consists of an encoder/decoder, scrambler/descrambler, wave-shaping transmitter, output driver, twisted-pair receiver with adaptive equalizer and baseline wander (BLW) correction, and clock and data recovery functions. The LAN8187/LAN8187i can be configured to support either the Media Independent Interface (MII) or the Reduced Media Independent Interface (RMII).

The LAN8187/LAN8187i is compliant with IEEE 802.3-2005 standards (MII Pins tolerant to 3.6V) and supports both IEEE 802.3-2005 -compliant and vendor-specific register functions. It contains a full-duplex 10-BASE-T/100BASE-TX transceiver and supports 10-Mbps (10BASE-T) operation on Category 3 and Category 5 unshielded twisted-pair cable, and 100-Mbps (100BASE-TX) operation on Category 5 unshielded twisted-pair cable.

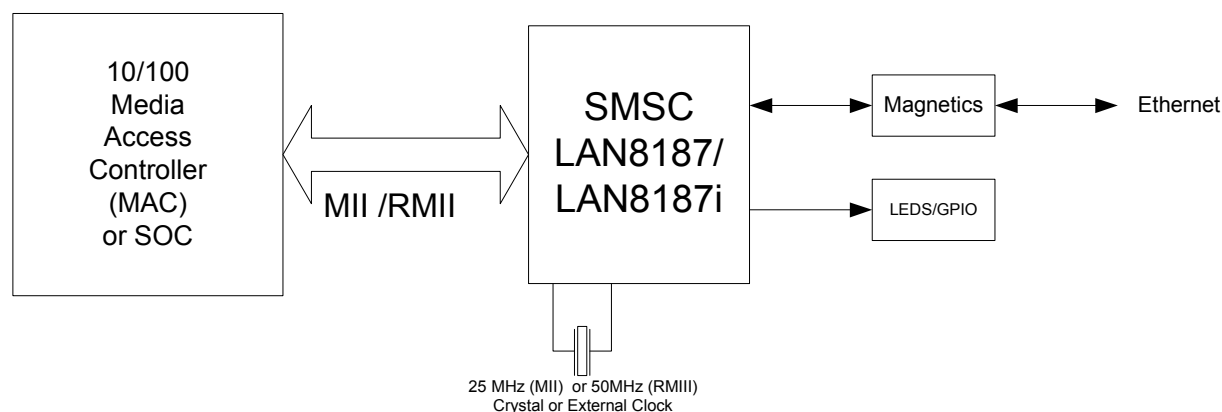


Figure 1 LAN8187/LAN8187i System Block Diagram

Hubs and switches with multiple integrated MACs and external PHYs can have a large pin count due to the high number of pins needed for each MII interface. An increasing pin count causes increasing cost.

The RMII interface is intended for use on Switch based ASICs or other embedded solutions requiring minimal pincount for ethernet connectivity. RMII requires only 6 pins for each MAC to PHY interface plus one common reference clock. The MII requires 16 pins for each MAC to PHY interface.

The SMSC LAN8187/LAN8187i is capable of running in RMII mode. Please refer to the RMII consortium for more information on the RMII standard <http://www.rmii-consort.com>.

The LAN8187/LAN8187i referenced throughout this document applies to both the commercial temperature and industrial temperature components. The LAN8187i refers to only the industrial temperature component.

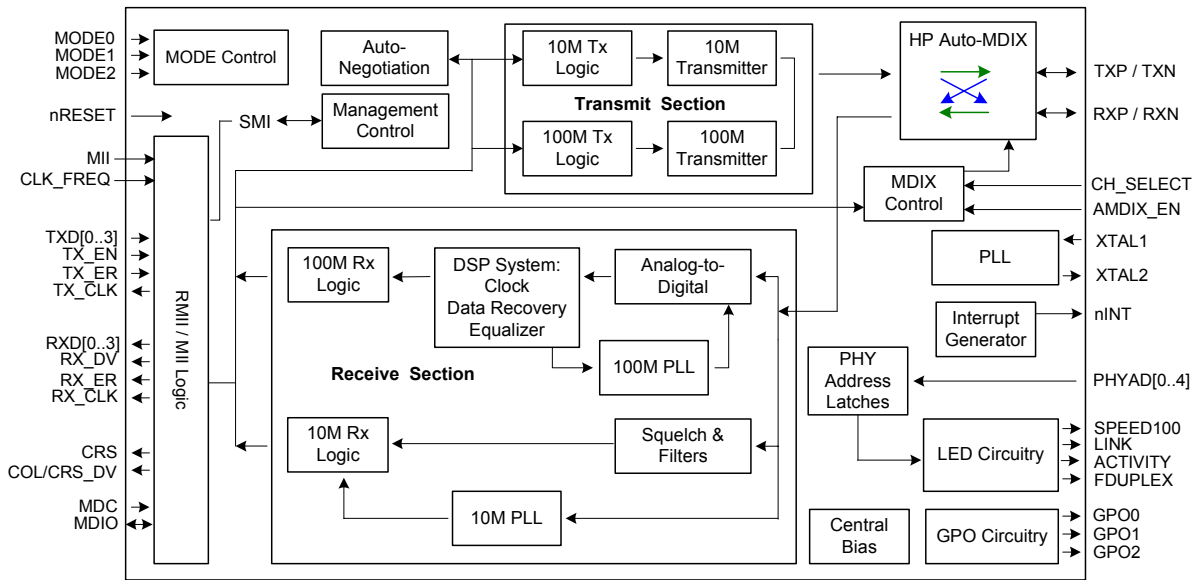


Figure 2 LAN8187/LAN8187i Architectural Overview

Pin Configuration

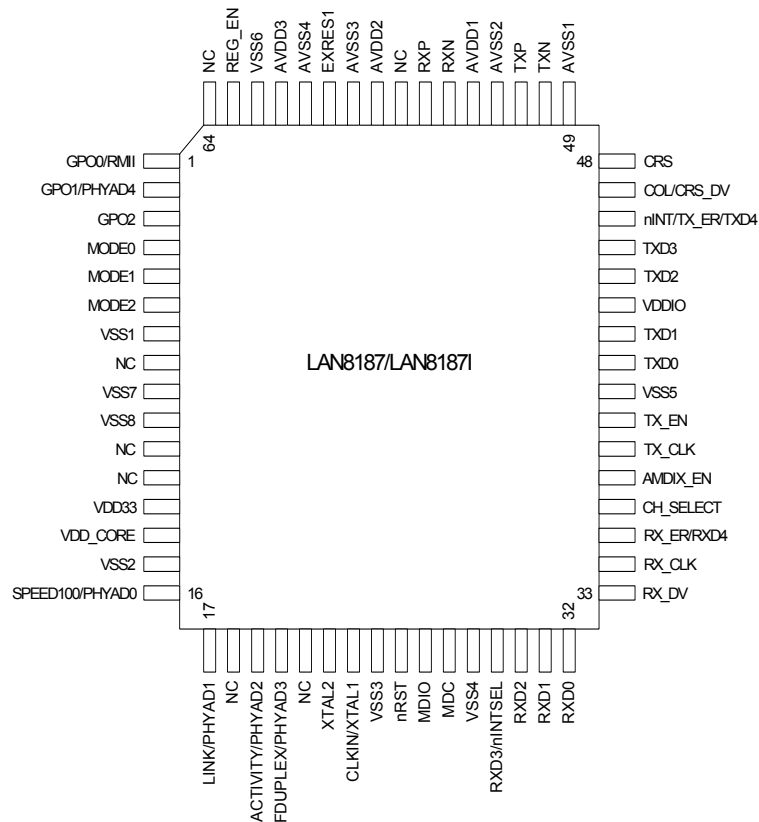


Figure 3 LAN8187/LAN8187i Package Pin Diagram (Top View)

**Table 1 LAN8187/LAN8187i 64-PIN TQFP Pinout**

PIN NO.	PIN NAME	PIN NO.	PIN NAME
1	GPO0/RMII	33	RX_DV
2	GPO1/PHYAD4	34	RX_CLK
3	GPO2	35	RX_ER/RXD4
4	MODE0	36	CH_SELECT
5	MODE1	37	AMDIX_EN
6	MODE2	38	TX_CLK
7	VSS1	39	TX_EN
8	NC	40	VSS5
9	VSS7	41	TXD0
10	VSS8	42	TXD1
11	NC	43	VDDIO
12	NC	44	TXD2
13	VDD33	45	TXD3
14	VDD_CORE	46	nINT/TX_ER/TXD4
15	VSS2	47	COL/CRS_DV
16	SPEED100/PHYAD0	48	CRS
17	LINK/PHYAD1	49	AVSS1
18	NC	50	TXN
19	ACTIVITY/PHYAD2	51	TXP
20	FDUPLEX/PHYAD3	52	AVSS2
21	NC	53	AVDD1
22	XTAL2	54	RXN
23	CLKIN/XTAL1	55	RXP
24	VSS3	56	NC
25	nRST	57	AVDD2
26	MDIO	58	AVSS3
27	MDC	59	EXRES1
28	VSS4	60	AVSS4
29	RXD3/nINTSEL	61	AVDD3
30	RXD2	62	VSS6
31	RXD1	63	REG_EN
32	RXD0	64	NC

Pin Definitions

This section describes the signals on each pin. When a lower case “n” is used at the beginning of the signal name, it indicates that the signal is active low. For example, nRST indicates that the reset signal is active low.

I/O Signals

- I Input. Digital LVCMOS levels.
- O Output. Digital LVCMOS levels.
- I/O Input or Output. Digital LVCMOS levels.

Note: The digital signals are not 5V tolerant. They are variable voltage from +1.6V to +3.6V.

- AI Input. Analog levels.
- AO Output. Analog levels.

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- AI Input. Analog levels.
- AO Output. Analog levels.

Table 2 MII Signals

SIGNAL NAME	TYPE	DESCRIPTION
TXD0	I	Transmit Data 0: Bit 0 of the 4 data bits that are accepted by the PHY for transmission.
TXD1	I	Transmit Data 1: Bit 1 of the 4 data bits that are accepted by the PHY for transmission.
TXD2	I	Transmit Data 2: Bit 2 of the 4 data bits that are accepted by the PHY for transmission Note: This signal should be grounded in RMII Mode.
TXD3	I	Transmit Data 3: Bit 3 of the 4 data bits that are accepted by the PHY for transmission. Note: This signal should be grounded in RMII Mode

Table 2 MII Signals (continued)

SIGNAL NAME	TYPE	DESCRIPTION
nINT/ TX_ER/ TXD4	I/O	<p>MII Transmit Error: When driven high, the 4B/5B encode process substitutes the Transmit Error code-group (/H/) for the encoded data word. This input is ignored in 10Base-T operation.</p> <p>MII Transmit Data 4: In Symbol Interface (5B Decoding) mode, this signal becomes the MII Transmit Data 4 line, the MSB of the 5-bit symbol code-group.</p> <p>Notes:</p> <ul style="list-style-type: none"> ■ This signal is not used in RMII Mode. ■ This signal is mux'd with nINT
TX_EN	I	<p>Transmit Enable: Indicates that valid data is presented on the TXD[3:0] signals, for transmission. In RMII Mode, only TXD[1:0] have valid data.</p>
TX_CLK	O	<p>Transmit Clock: 25MHz in 100Base-TX mode. 2.5MHz in 10Base-T mode.</p> <p>Note: This signal is not used in RMII Mode</p>
RXD0	O	<p>Receive Data 0: Bit 0 of the 4 data bits that are sent by the PHY in the receive path.</p>
RXD1	O	<p>Receive Data 1: Bit 1 of the 4 data bits that are sent by the PHY in the receive path.</p>
RXD2	O	<p>Receive Data 2: Bit 2 of the 4 data bits that sent by the PHY in the receive path.</p> <p>Note: This signal is not used in RMII Mode.</p>
RXD3/ nINTSEL	O	<p>Receive Data 3: Bit 3 of the 4 data bits that sent by the PHY in the receive path.</p> <p>nINTSEL: On power-up or external reset, the mode of the nINT/TXER/TXD4 pin is selected.</p> <ul style="list-style-type: none"> ■ When floated or pulled to VDDIO, nINT is selected (default). <p>Notes:</p> <ul style="list-style-type: none"> ■ RXD3 is not used in RMII Mode ■ If the nINT/TXER/TXD4 pin is configured for nINT mode, it needs a pull-up resistor to VDDIO.
RX_ER/ RXD4	I/O	<p>Receive Error: Asserted to indicate that an error was detected somewhere in the frame presently being transferred from the PHY.</p> <p>MII Receive Data 4: In Symbol Interface (5B Decoding) mode, this signal is the MII Receive Data 4 signal, the MSB of the received 5-bit symbol code-group. Unless configured in this mode, the pin functions as RX_ER.</p> <p>Notes:</p> <ul style="list-style-type: none"> ■ This pin has an internal pull-down resistor, and must not be high during reset. The RX_ER signal is optional in RMII Mode.
RX_CLK	O	<p>Receive Clock: 25MHz in 100Base-TX mode. 2.5MHz in 10Base-T mode.</p> <p>Notes:</p> <ul style="list-style-type: none"> ■ This signal is not used in RMII Mode

Table 2 MII Signals (continued)

SIGNAL NAME	TYPE	DESCRIPTION
COL/CRS_DV	O	<p>MII Collision Detect: Asserted to indicate detection of collision condition.</p> <p>RMII CRS_DV (Carrier Sense/Receive Data Valid) Asserted to indicate when the receive medium is non-idle. When a 10BT packet is received, CRS_DV is asserted, but RXD[1:0] is held low until the SFD byte (10101011) is received. In 10BT, half-duplex mode, transmitted data is not looped back onto the receive data pins, per the RMII standard.</p>

Table 3 LED Signals

SIGNAL NAME	TYPE	DESCRIPTION
CRS	O	Carrier Sense: Indicates detection of carrier.
RX_DV	O	<p>Receive Data Valid: Indicates that recovered and decoded data nibbles are being presented on RXD[3:0].</p> <p>Note: This signal is not used in RMII Mode.</p>
SPEED100/ PHYAD0	I/O	<p>LED1 – SPEED100 indication. Active indicates that the selected speed is 100Mbps. Inactive indicates that the selected speed is 10Mbps.</p> <p>Note: This signal is mux'd with PHYAD0</p>
LINK/ PHYAD1	I/O	<p>LED2 – LINK ON indication. Active indicates that the Link (100Base-TX or 10Base-T) is on.</p> <p>Note: This signal is mux'd with PHYAD1</p>
ACTIVITY/ PHYAD2	I/O	<p>LED3 – ACTIVITY indication. Active indicates that there is Carrier sense (CRS) from the active PMD.</p> <p>Note: This signal is mux'd with PHYAD2</p>
FDUPLEX/ PHYAD3	I/O	<p>LED4 – DUPLEX indication. Active indicates that the PHY is in full-duplex mode.</p> <p>Note: This signal is mux'd with PHYAD3</p>

Table 4 Management Signals

SIGNAL NAME	TYPE	DESCRIPTION
MDIO	I/O	Management Data Input/OUTPUT: Serial management data input/output.
MDC	I	Management Clock: Serial management clock.

Table 5 Boot Strap Configuration Inputs (Note 1)

SIGNAL NAME	TYPE	DESCRIPTION
GPO1/ PHYAD4	I/O	PHY Address Bit 4: set the default address of the PHY. This signal is mux'd with GPO1
FDUPLEX/ PHYAD3	I/O	PHY Address Bit 3: set the default address of the PHY. Note: This signal is mux'd with FDUPLEX
ACTIVITY/ PHYAD2	I/O	PHY Address Bit 2: set the default address of the PHY. Note: This signal is mux'd with ACTIVITY
LINK/ PHYAD1	I/O	PHY Address Bit 1: set the default address of the PHY. Note: This signal is mux'd with LINK
SPEED100/ PHYAD0	I/O	PHY Address Bit 0: set the default address of the PHY. Note: This signal is mux'd with SPEED100
MODE2	I	PHY Operating Mode Bit 2: set the default MODE of the PHY.
MODE1	I	PHY Operating Mode Bit 1: set the default MODE of the PHY.
MODE0	I	PHY Operating Mode Bit 0: set the default MODE of the PHY.
REG_EN	I	Regulator Enable: Internal +1.8V regulator enable: VDDIO – Enables internal regulator. VSS– Disables internal regulator.
AMDIX_EN	I	HP Auto-MDIX Enable: This pin is used to manually disable the HP Auto-MDIX function. This can be bypassed using the internal register 27 bit 15. (VDDIO or Floating) – Enables HP Auto-MDIX. VSS – Disables HP Auto-MDIX
CH_SELECT	I	Channel Select: This pin is used in conjunction with the AMDIX_EN pin above to manually select the channel to transmit and receive on. (VDDIO or Floating) – MDIX - TX pair receives RX pair transmits. 0V – MDI -TX pair transmits RX pair receives.
GPO0/RMII	I/O	General Purpose Output 0 – General Purpose Output signal. Driven by bits in registers 27 and 31. RMII – MII/RMII mode selection is latched on the rising edge of the internal reset (nreset) based on the following strapping: Float the GPO0 pin for MII mode or pull-high with an external Pull-up resistor to VDDIO to set the device in RMII mode.

Note 1 On nRST transition high, the PHY latches the state of the configuration pins in this table.

Table 6 General Signals

SIGNAL NAME	TYPE	DESCRIPTION
nINT	I/O	LAN Interrupt – Active Low output. Place a pull-up external resistor to VCC 3.3V. Note: This signal is mux'd with TX_ER/TXD4
nRST	I	External Reset – input of the system reset. This signal is active LOW.

Table 6 General Signals (continued)

SIGNAL NAME	TYPE	DESCRIPTION
CLKIN/XTAL1	I	Clock Input – 25 Mhz or 50 MHz external clock or crystal input. In MII mode, this signal is the 25 MHz reference input clock In RMII mode, this signal is the 50 MHz reference input clock which is typically also driven to the RMII compliant Ethernet MAC clock input.
XTAL2	O	Clock Output – 25 MHz crystal output.
GPO2	O	General Purpose Output 2 – General Purpose Output signal Driven by bits in registers 27 and 31.
GPO1	O	General Purpose Output 1 – General Purpose Output signal Driven by bits in registers 27 and 31. This signal is mux'd with PHYAD4.
GPO0/RMII	I/O	General Purpose Output 0 – General Purpose Output signal. Driven by bits in registers 27 and 31. RMII – MII/RMII mode selection is latched on the rising edge of nRST based on the following strapping: Float the GPO0 pin for MII mode or pull-high with an external resistor to VDDIO to set the device in RMII mode.

Table 7 10/100 Line Interface

SIGNAL NAME	TYPE	DESCRIPTION
TXP	AO	Transmit Data: 100Base-TX or 10Base-T differential transmit outputs to magnetics.
TXN	AO	Transmit Data: 100Base-TX or 10Base-T differential transmit outputs to magnetics.
RXP	AI	Receive Data: 100Base-TX or 10Base-T differential receive inputs from magnetics.
RXN	AI	Receive Data: 100Base-TX or 10Base-T differential receive inputs from magnetics.

Table 8 Analog References

SIGNAL NAME	TYPE	DESCRIPTION
EXRES1	AI	Connects to reference resistor of value 12.4K-Ohm, 1% connected as described in the Analog Layout Guidelines.

**Table 9 No Connect Signals**

SIGNAL NAME	TYPE	DESCRIPTION
NC		No Connect

Table 10 Power Signals

SIGNAL NAME	TYPE	DESCRIPTION
AVDD[1-3]	POWER	+3.3V Analog Power
AVSS[1-4]	POWER	Analog Ground
VDD_CORE	POWER	+1.8V (Core voltage) - 1.8V regulator output for digital circuitry on chip. Place a 0.1uF capacitor near this pin and connect the capacitor from this pin to ground. In parallel, place a 4.7uF +/-20% low ESR capacitor near this pin and connect the capacitor from this pin to ground. X5R or X7R ceramic capacitors are recommended since they exhibit an ESR lower than 0.1ohm at frequencies greater than 10kHz.
VDD33	POWER	+3.3V Digital Power
VDDIO	POWER	+1.6V to +3.6V Variable I/O Pad Power
VSS[1-8]	POWER	Digital Ground (GND)

Package Outline

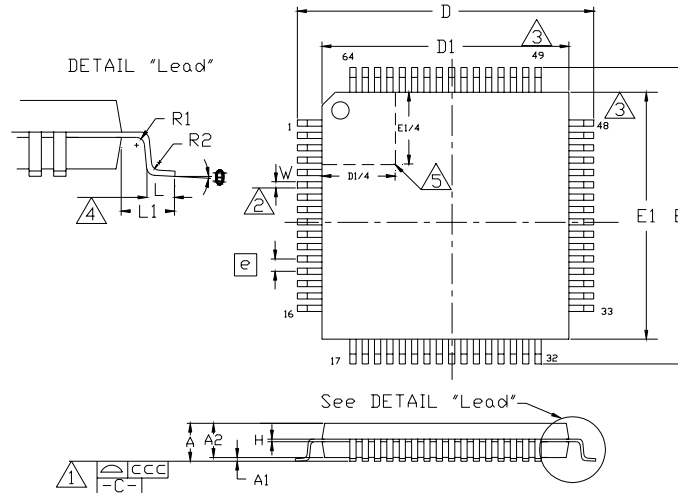


Figure 4 64 Pin TQFP Package Outline, 10X10X1.4 Body, 12x12 mm Footprint

Table 11 64 Pin TQFP Package Parameters

	MIN	NOMINAL	MAX	REMARKS
A	~	~	1.60	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	1.35	~	1.45	Body Thickness
D	11.80	~	12.20	X Span
D1	9.80	~	10.20	X body Size
E	11.80	~	12.20	Y Span
E1	9.80	~	10.20	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length
L1	~	1.00	~	Lead Length
e	0.50 Basic			Lead Pitch
θ	0°	~	7°	Lead Foot Angle
W	0.17	0.22	0.27	Lead Width
R	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

Notes:

1. Controlling Unit: millimeter.
2. Tolerance on the true position of the leads is ± 0.04 mm maximum.
3. Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25 mm per side.
4. Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
5. Details of pin 1 identifier are optional but must be located within the zone indicated.